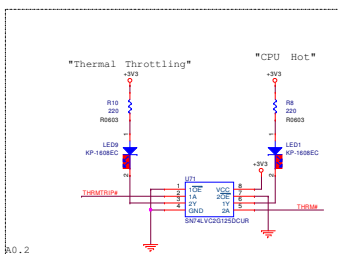
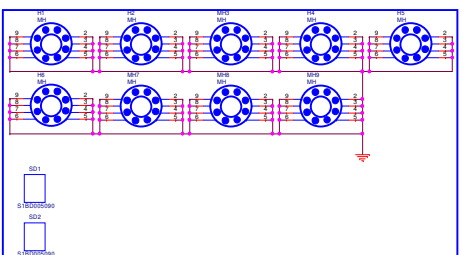
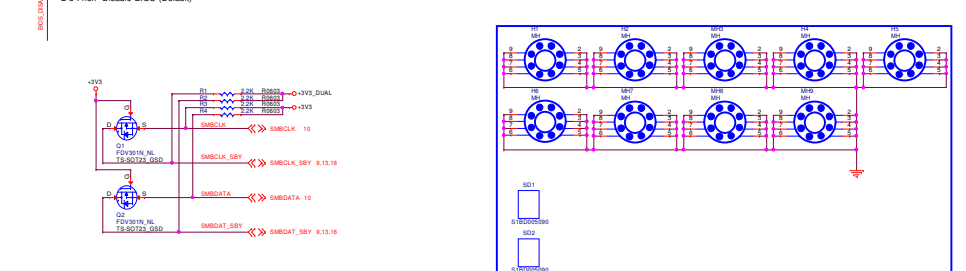
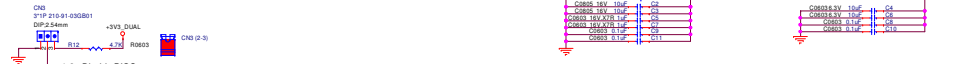
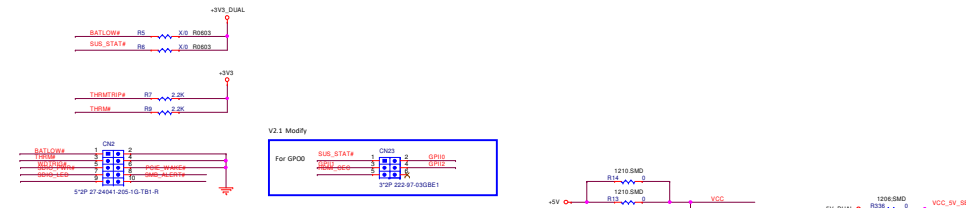
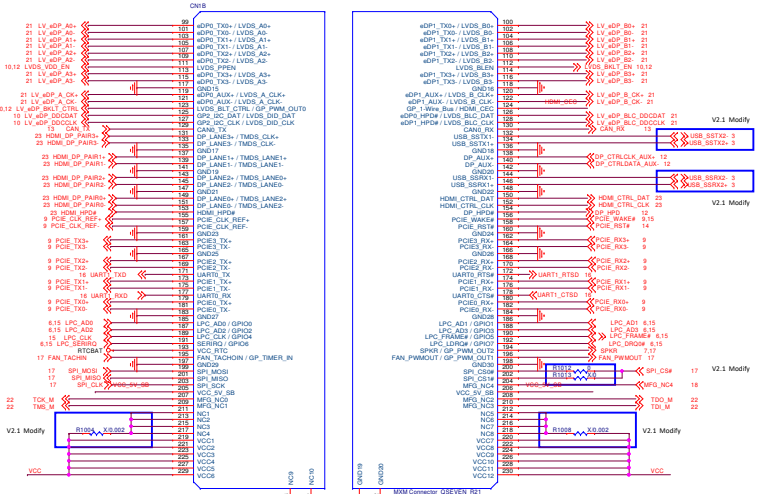
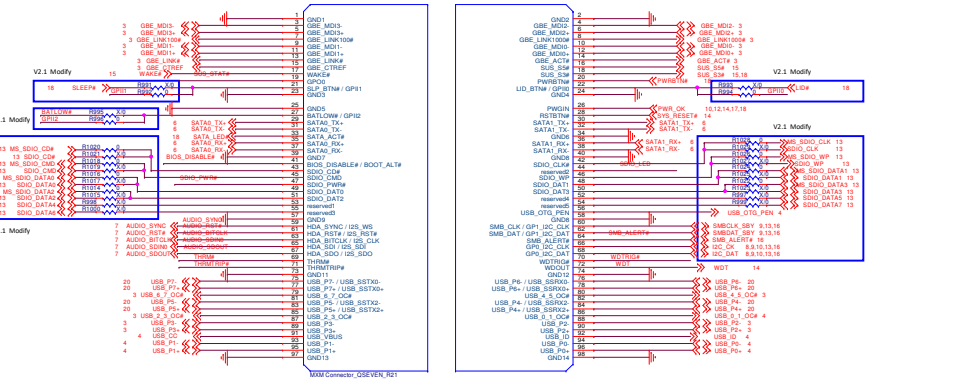
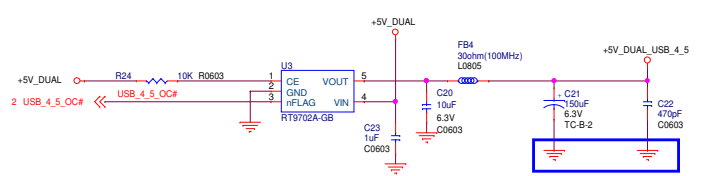
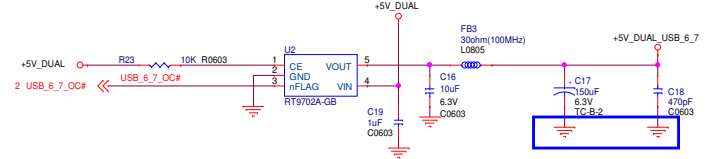
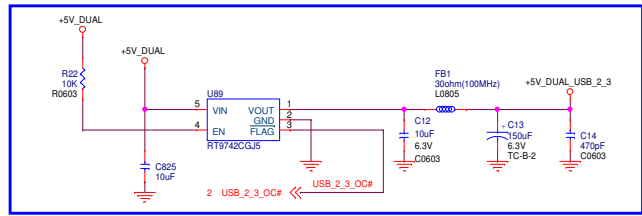


Page	Index
1	Cover Sheet
2	MXM
3	LAN-RJ45 + USB2.0
4	USB2.0 + USB3.0
5	USB3.0 Redriver
6	SATA
7	Audio
8	F-AUDIO
9	PCIe x4 Slots
10	LVDS
11	VGA
12	DP Port + eDP Port
13	CANBUS / SMBUS / I2C / SD
14	RESET + PWROK
15	SIO Card SLOT
16	Serial port + LPC
17	SPI + Buzzer + FAN + RTC
18	ATX Power + Front Panel
19	+5V_DUAL/+3V3_DUAL/5V
20	USB3.0 Switch
21	LVDS/eDP Switch
22	LPC 80H
23	DP/HDMI Switch
24	Revision History



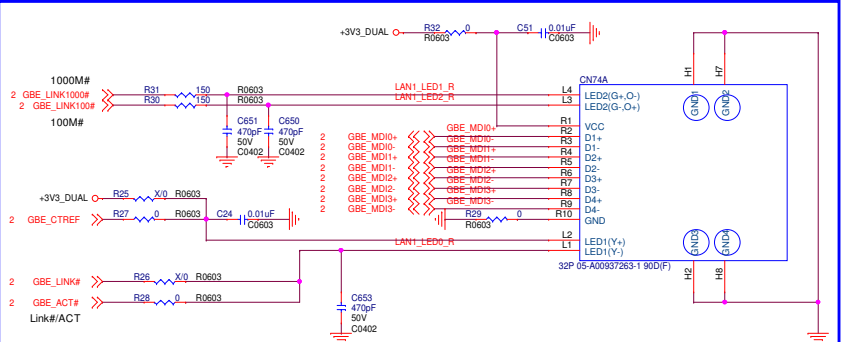
V2.1 Modify



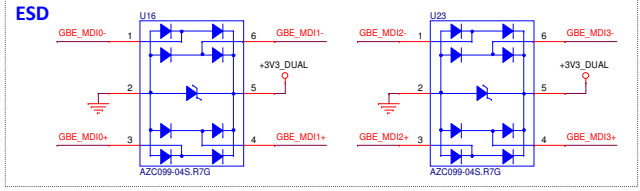
V2.1 Modify

V2.1 Modify

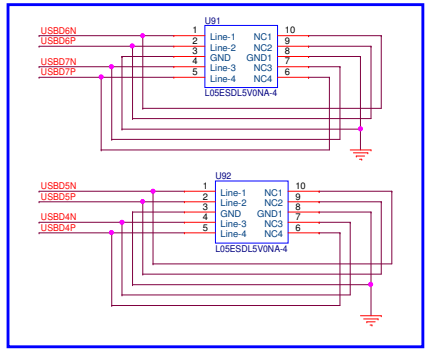
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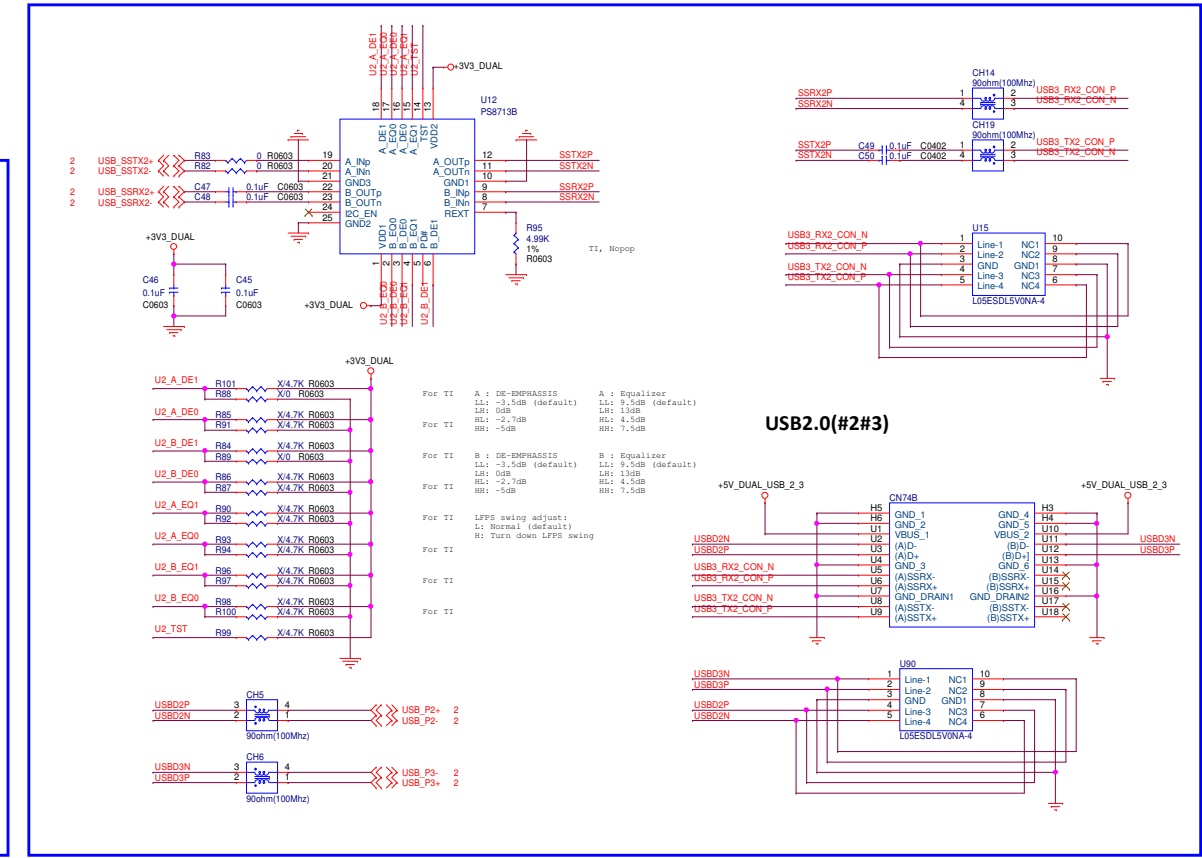
Place Caps close to the LEDs (Optional for EMI Suppression. Default 470pF, value may vary)



V2.1 Modify

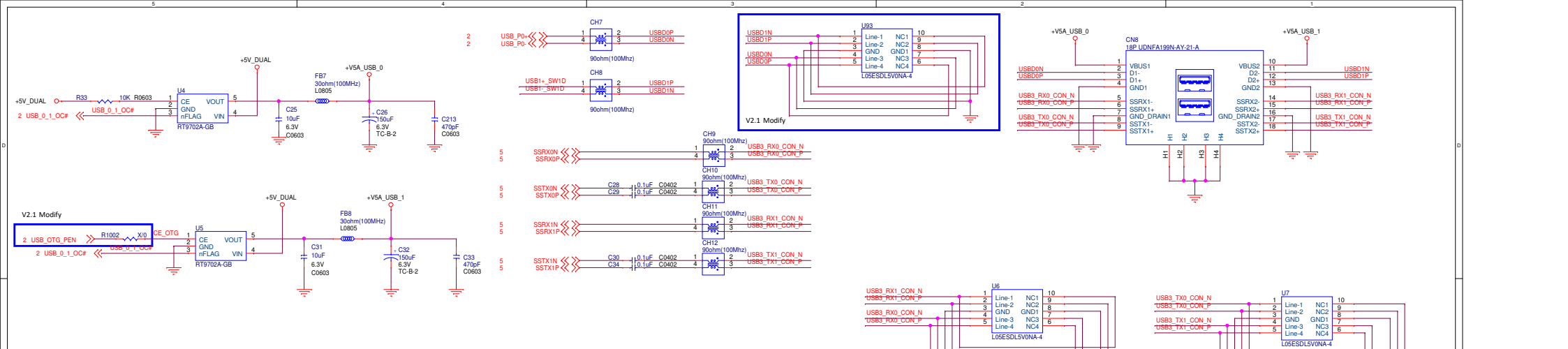


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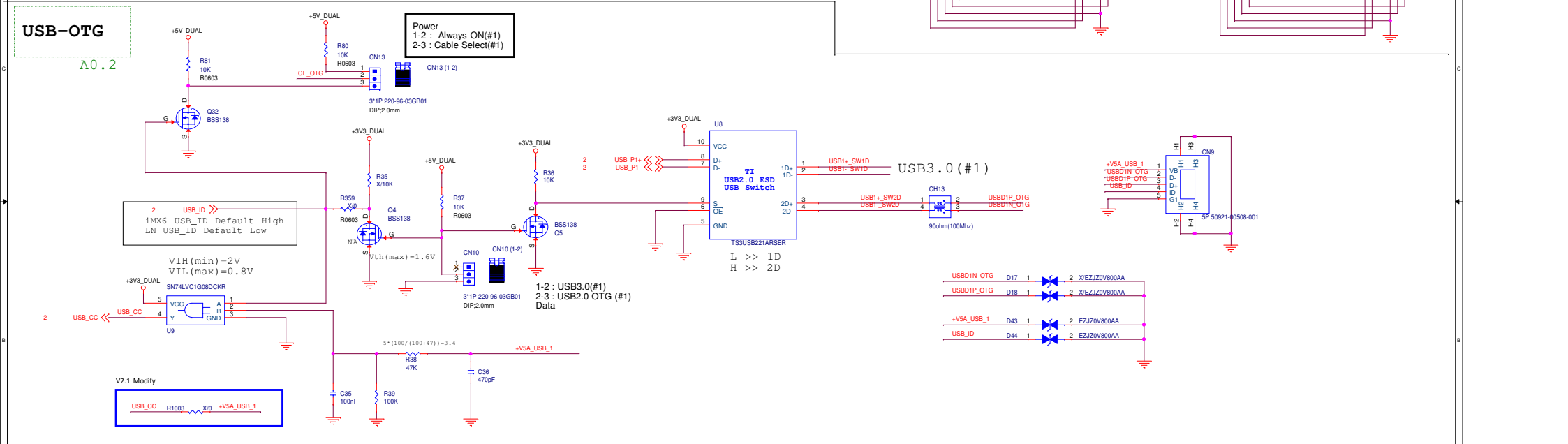
USB2.0(#4#5#6#7)

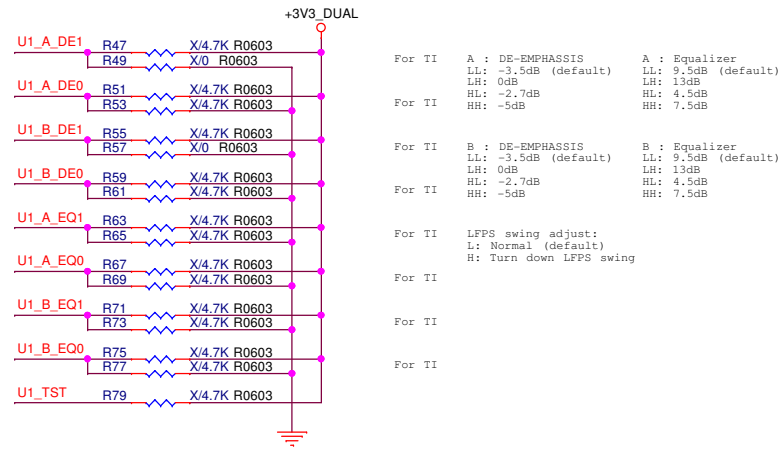
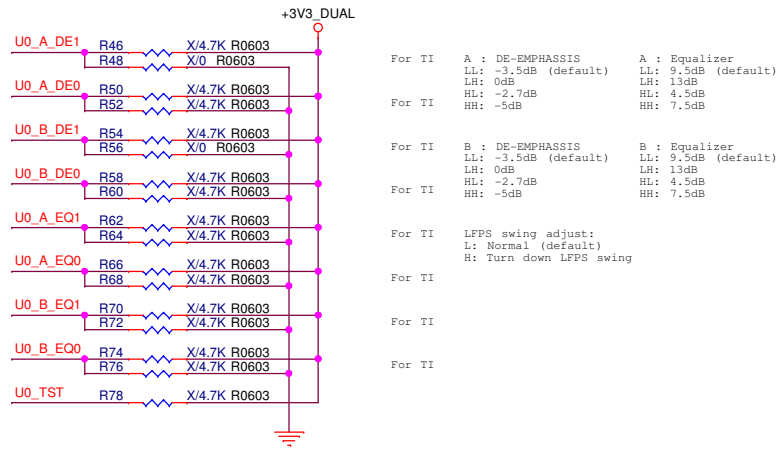
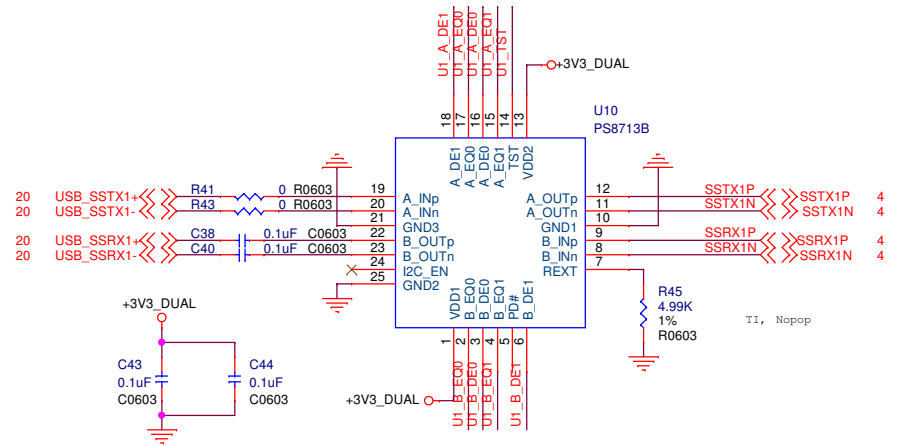
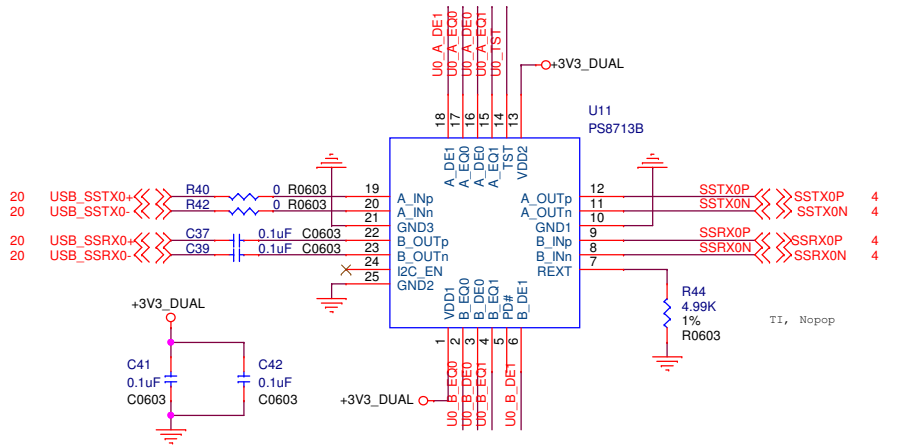
USB2.0(#2#3)




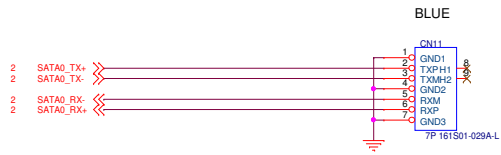
USB-OTG
A0.2

Power
1-2 : Always ON(#1)
2-3 : Cable Select(#1)

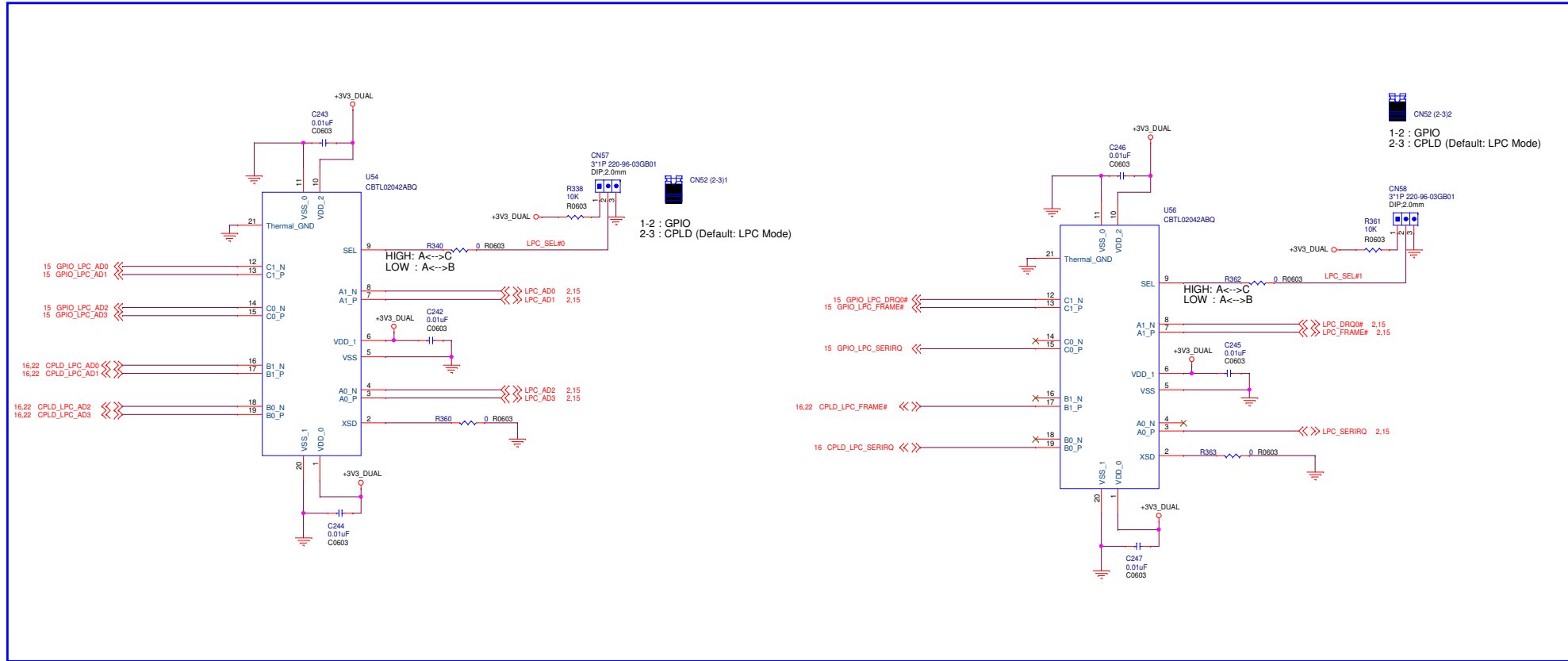


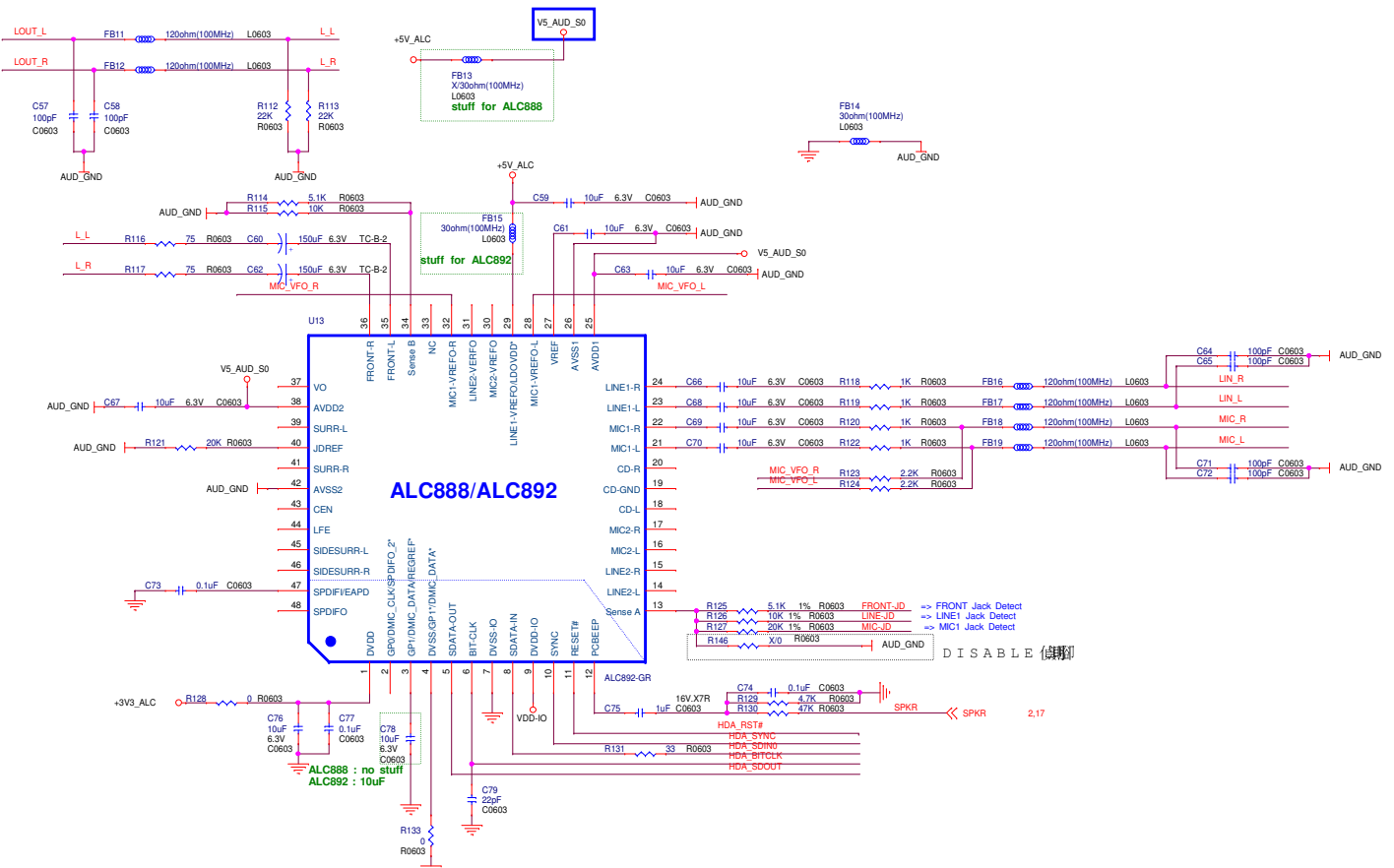


		AAEON Technology INC.	
		Title USB3.0 Redriver	
Size B	Document Number ECB-970	Rev A2.0_0_0	
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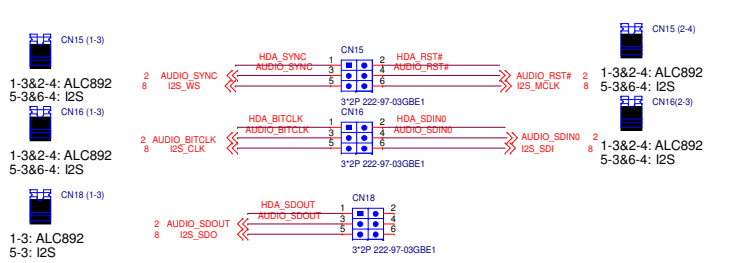


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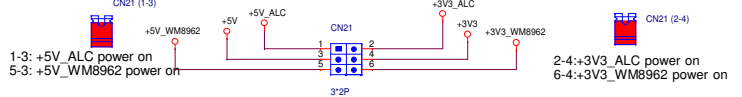




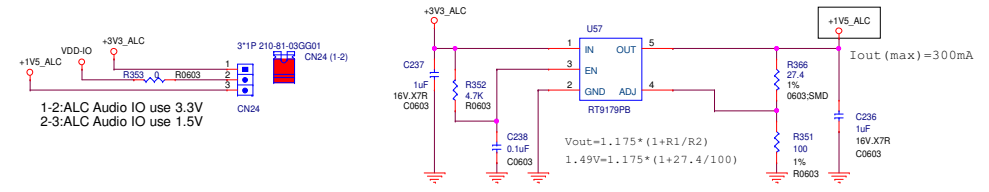
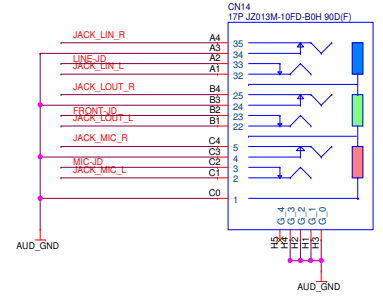
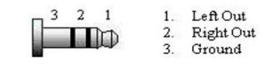
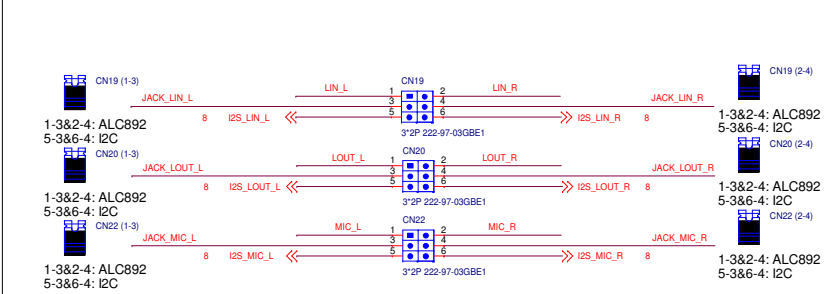
AUDIO INPUT SEL

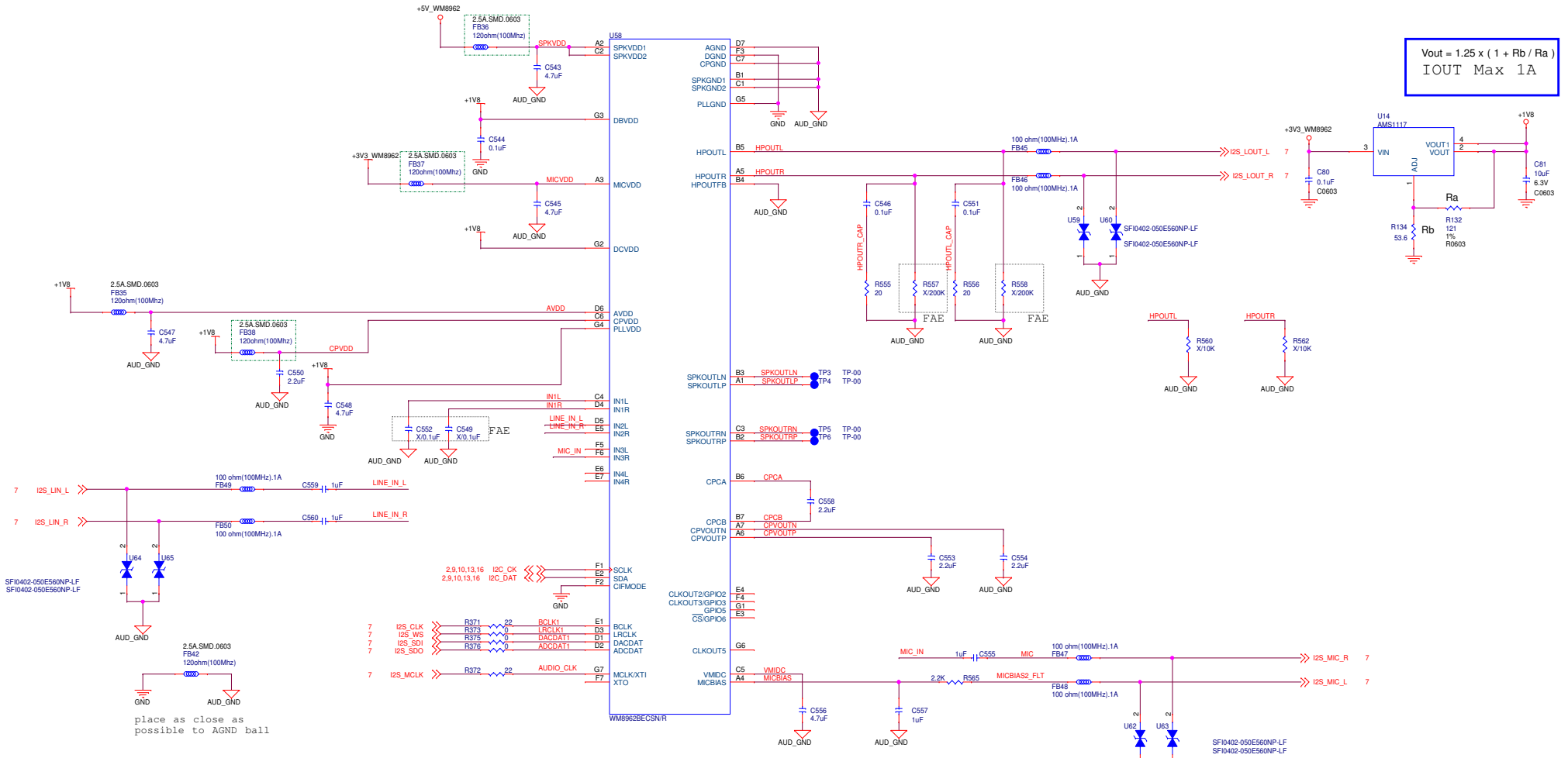


ALC Power



AUDIO OUTPUT SEL

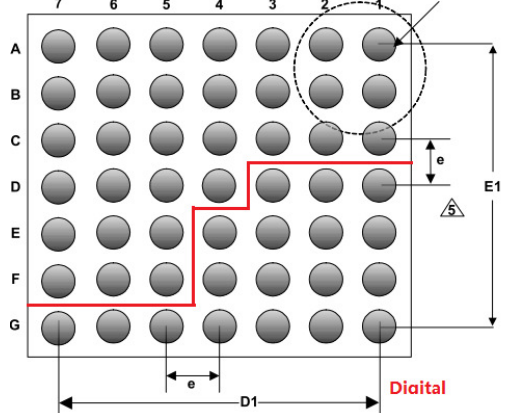




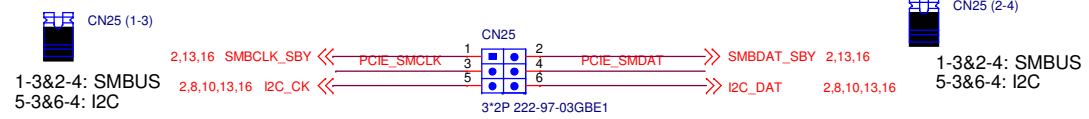
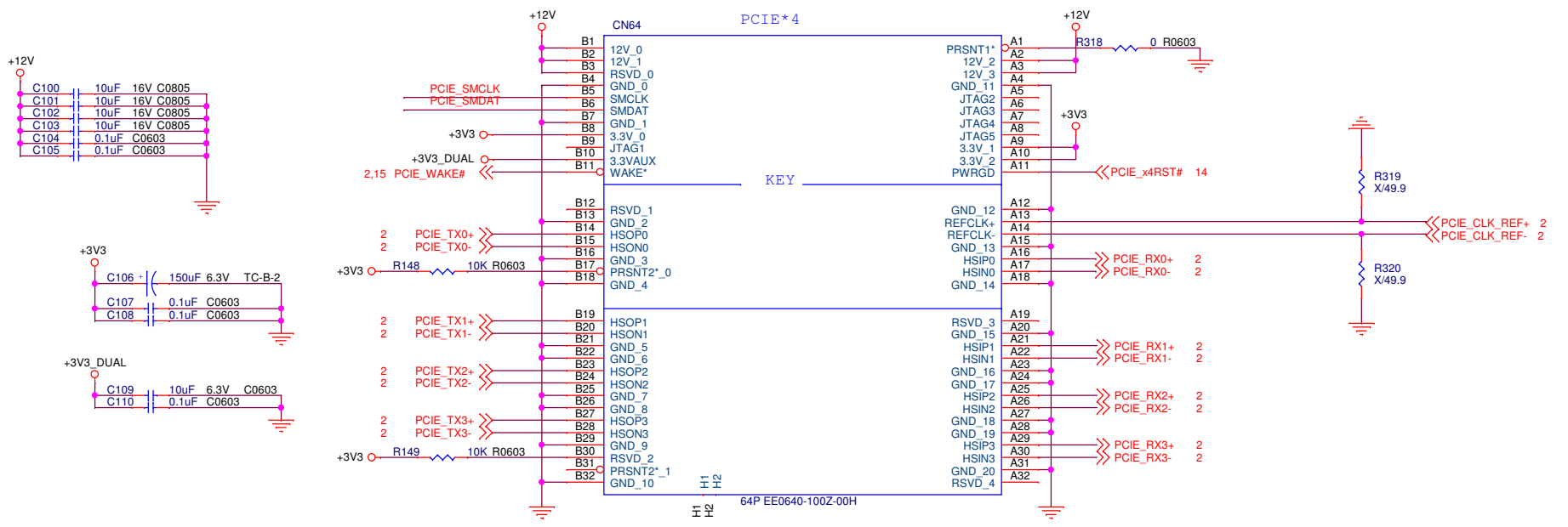
$$V_{out} = 1.25 \times (1 + R_b / R_a)$$

$$I_{OUT} \text{ Max } 1A$$

Analog **DETAIL 1**



BOTTOM VIEW



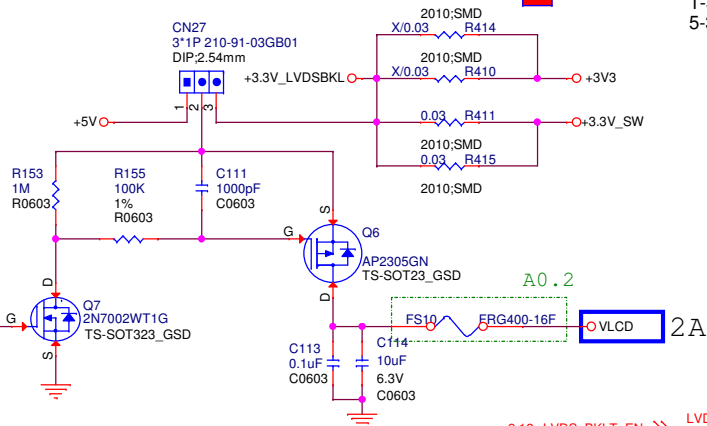
	x1		x4/x8		x16	
Standard height	10 W ¹ (max)	25 W ¹ (max)	25 W (max)	25 W ² (max)	75 W ^{2,4} (max)	75 W ^{2,4} (max)
Low profile card ³	10 W (max)	25 W (max)	25 W (max)	25 W (max)		

Power Rail	10 W Slot	25 W Slot	75 W Slot
+3.3V			
Voltage tolerance	± 9% (max)	± 9% (max)	± 9% (max)
Supply Current	3.0 A (max)	3.0 A (max)	3.0 A (max)
Capacitive Load	1000 μF (max)	1000 μF (max)	1000 μF (max)
+12V			
Voltage tolerance	± 8%	± 8%	± 8%
Supply Current	0.5 A	2.1 A (max)	5.5 A (max)
Capacitive Load	300 μF (max)	1000 μF (max)	2000 μF (max)
+3.3Vaux			
Voltage tolerance	± 9% (max)	± 9% (max)	± 9% (max)
Supply Current			
Wakeup Enabled	375 mA (max)	375 mA (max)	375 mA (max)
Non-wakeup Enabled	20 mA (max)	20 mA (max)	20 mA (max)
Capacitive Load	150 μF (max)	150 μF (max)	150 μF (max)

		AAEON Technology INC.	
		Title PCIe x1 Slots	
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LVDS Operating Voltage Selection

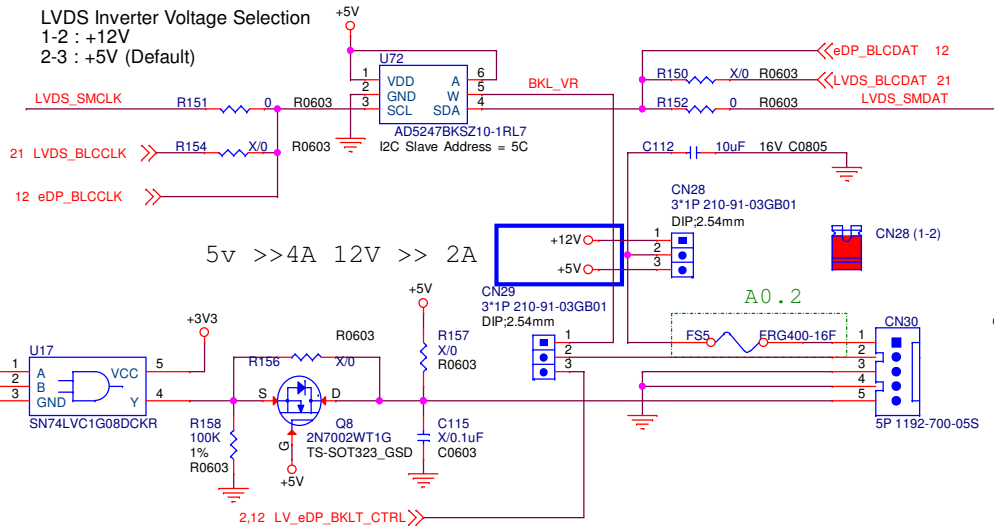
1-2 : +5V
2-3 : +3.3V (Default)



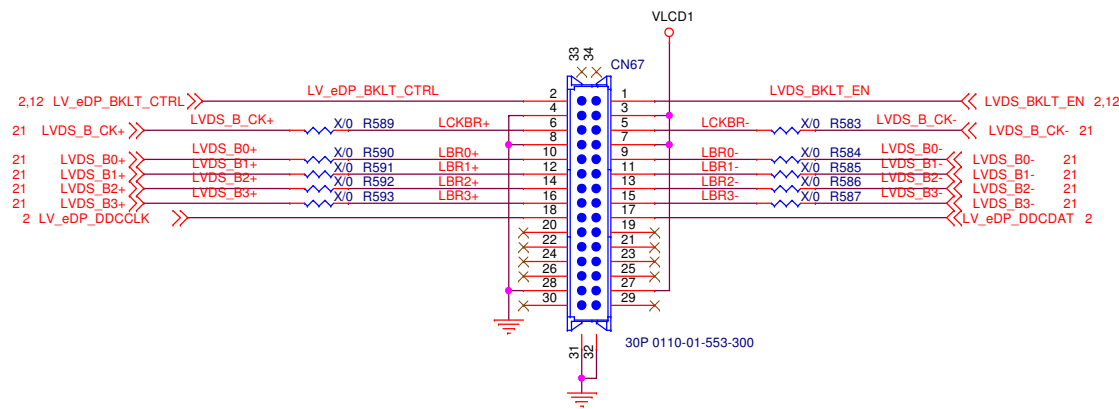
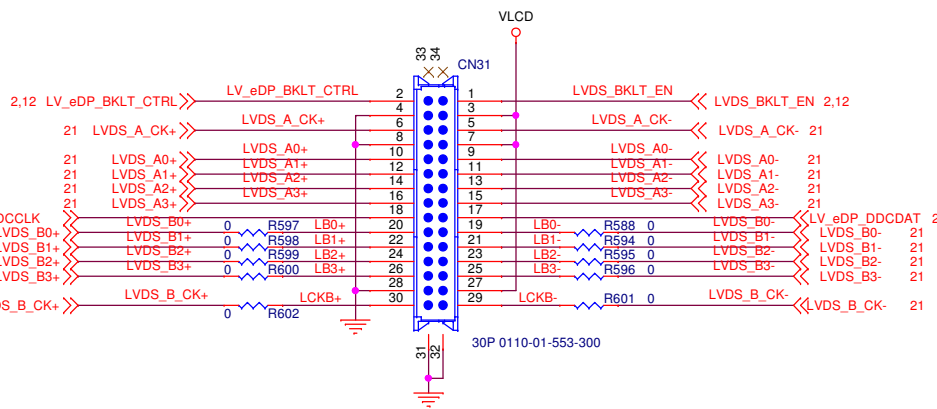
1-3&2-4: SMBUS
5-3&6-4: I2C


LVDS Inverter Voltage Selection

1-2 : +12V
2-3 : +5V (Default)

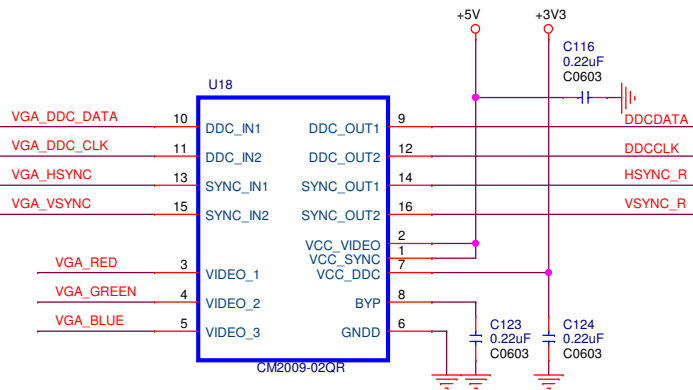
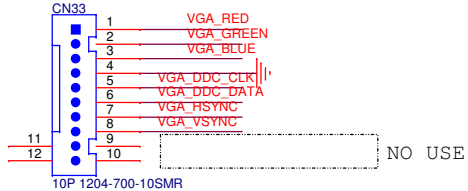
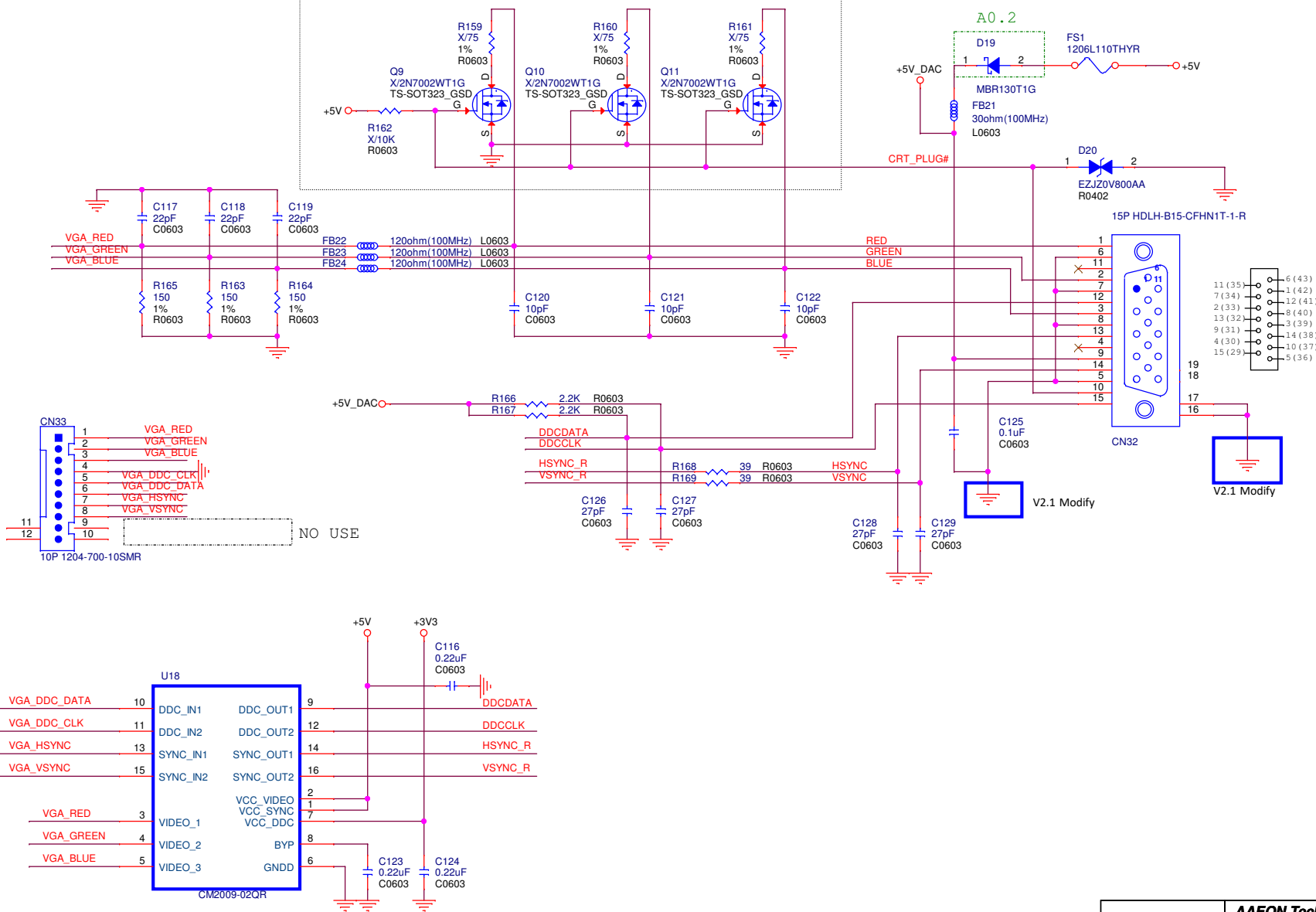



5v >>4A 12V >> 2A



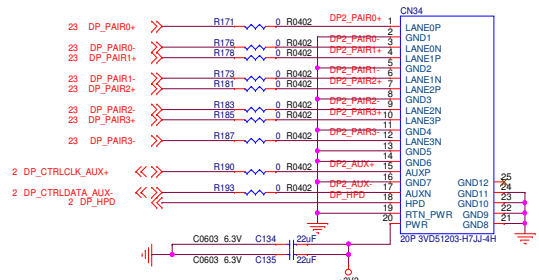
		AEEON Technology INC.	
		Title LVDS	
Size B	Document Number ECB-970	Rev A2.0_0.0	
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CRT Always On Circuit

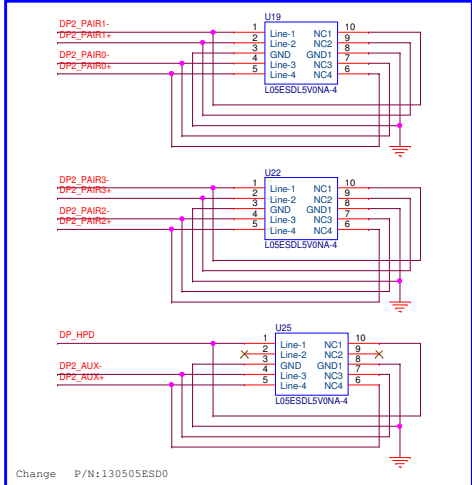


 AAEON [®] An ASUS Company		AAEON Technology INC.	
		Title VGA_DVI	
Size B	Document Number ECB-970		Rev A2.0_0_0
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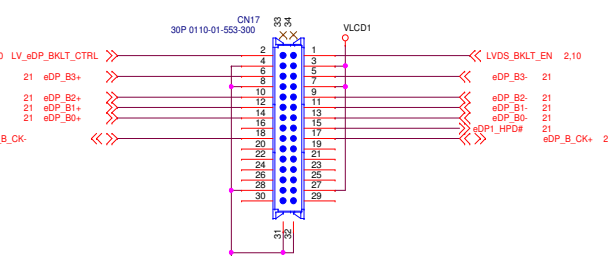
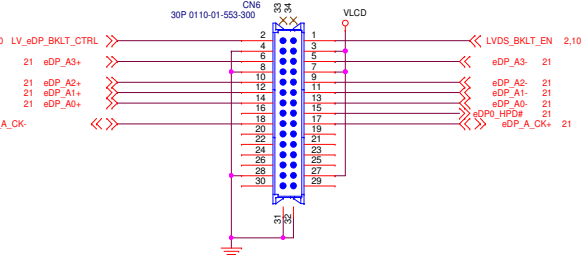
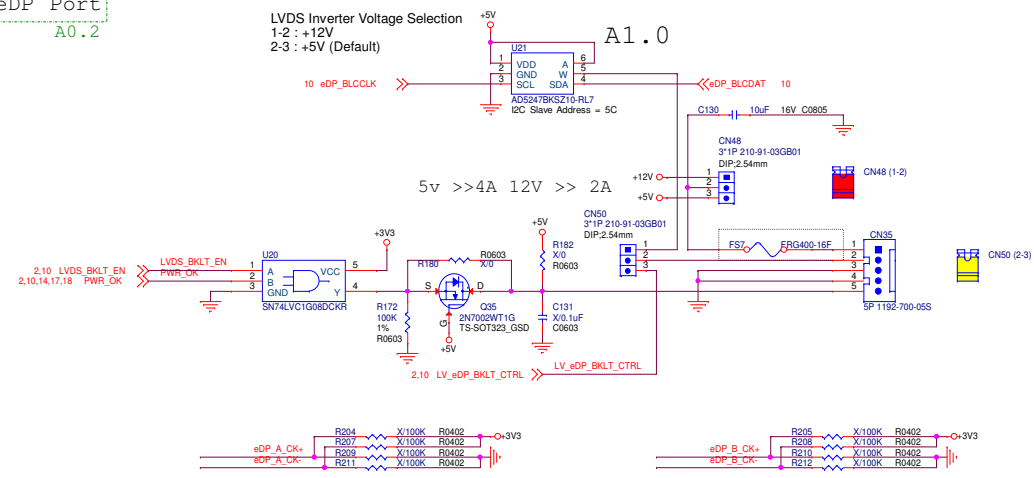
DP Port



V2.1 Modify

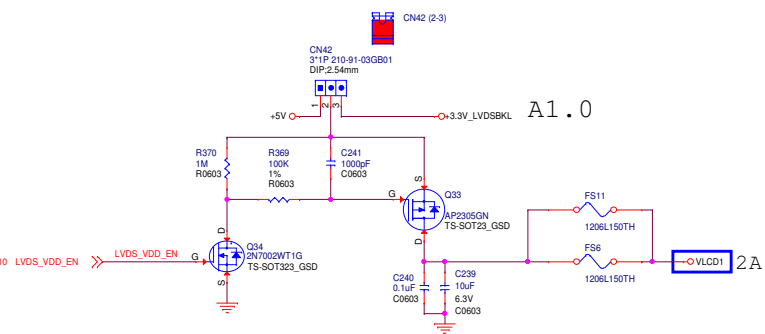


eDP Port
A0.2



PIN	LVDS	eDP	PIN	LVDS	eDP
1	LVD_BKLTEN	EDP_BKLEN	2	LVD_BKCTL	EDP_BKCTL
3	VLCD		4	GND	
5	LVD_A_CLKN	eDP_TXN3	6	LVD_A_CLKP	eDP_TXP3
7	VLCD		8	GND	
9	LVD_A_TXN0	eDP_TXN2	10	LVD_A_TXP0	eDP_TXP2
11	LVD_A_TXN1	eDP_TXN1	12	LVD_A_TXP1	eDP_TXP1
13	LVD_A_TXN2	eDP_TXN0	14	LVD_A_TXP2	eDP_TXP0
15	LVD_A_TXN3	None	16	LVD_A_TXP3	eDP_HPDP#
17	LVD_DDC_SDA	eDP_AUX_N	18	LVD_DDC_SCL	eDP_AUX_P
19	LVD_B_TXN0		20	LVD_B_TXP0	
21	LVD_B_TXN1		22	LVD_B_TXP1	
23	LVD_B_TXN2		24	LVD_B_TXP2	
25	LVD_B_TXN3		26	LVD_B_TXP3	
27	VLCD		28	GND	
29	LVD_B_CLKN		30	LVD_B_CLKP	

LVDS Operating Voltage Selection
1-2 : +5V
2-3 : +3.3V (Default)



AEEON Technology INC.

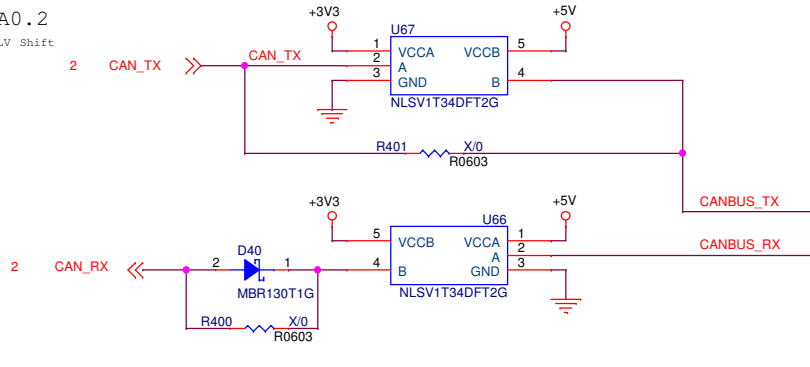
Rev: **HDMI**

Doc: **ECB-970**

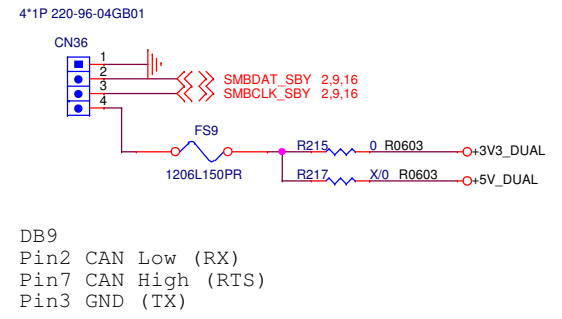
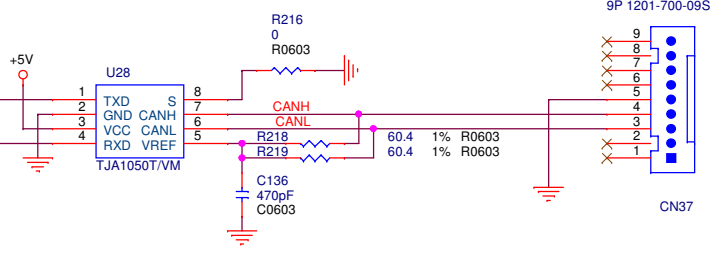
Rev: **A2.0_0**

Date: Friday, March 09, 2018 | Sheet: 12 of 24

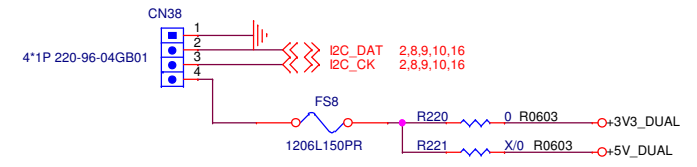
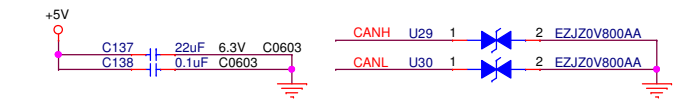
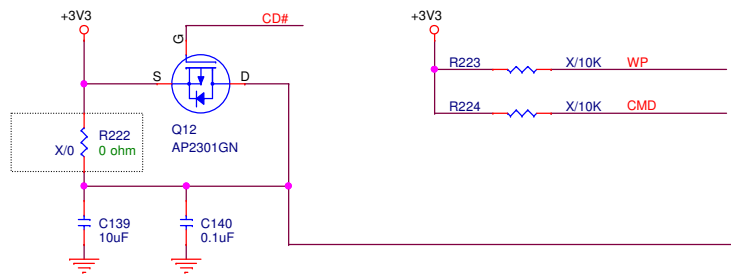
A0.2
LV Shift



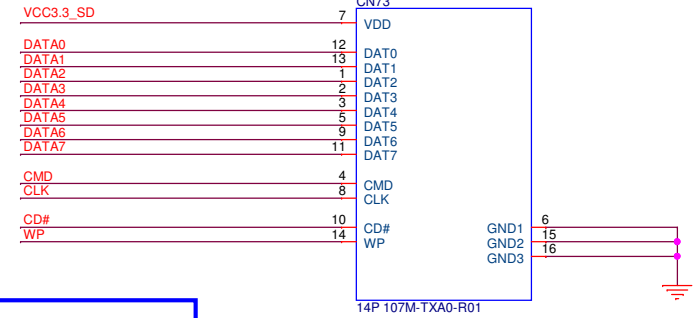
A1.0



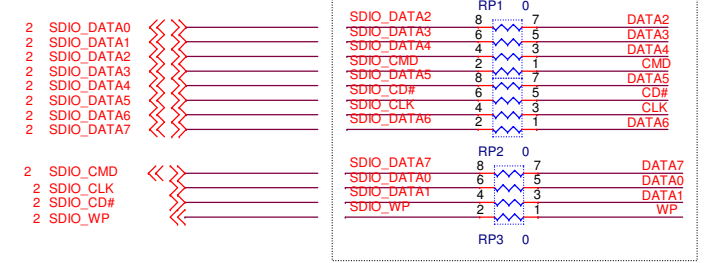
DB9
Pin2 CAN Low (RX)
Pin7 CAN High (RTS)
Pin3 GND (TX)



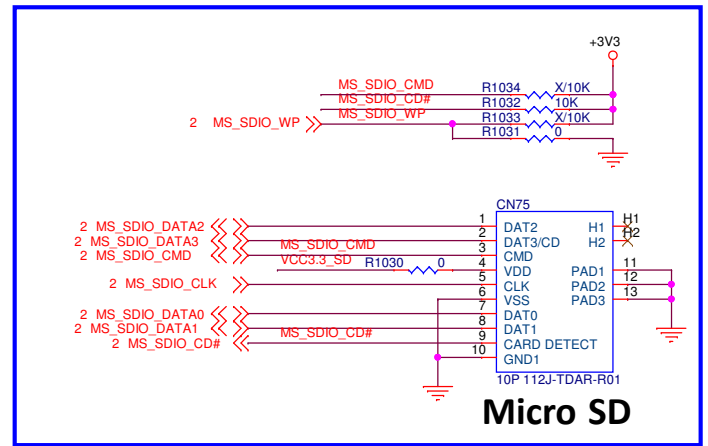
A0.2
1654914200



swap

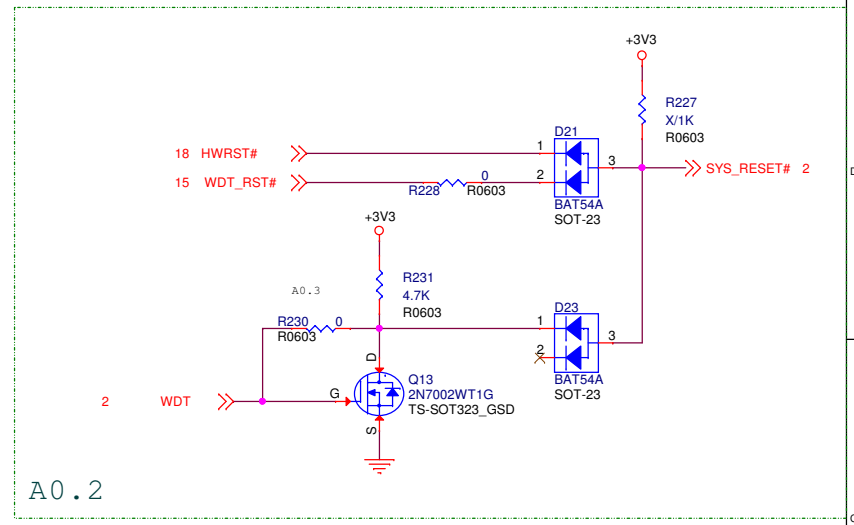
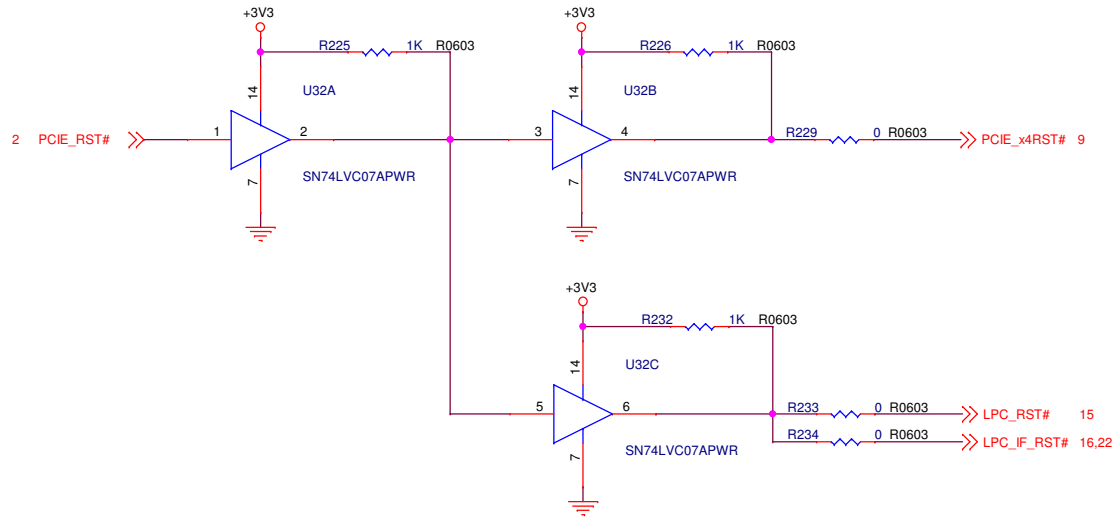


V2.1 Modify

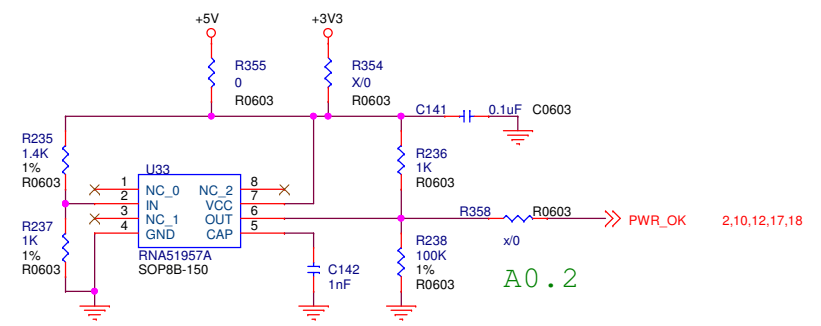


Micro SD

Title P13 CANBUS / SMBUS / I2C / SD		
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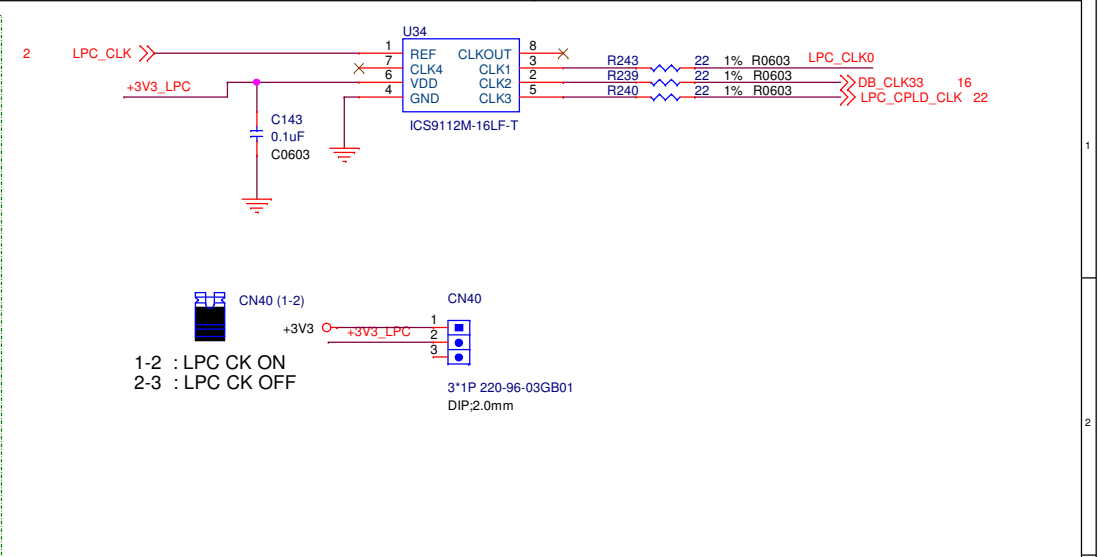
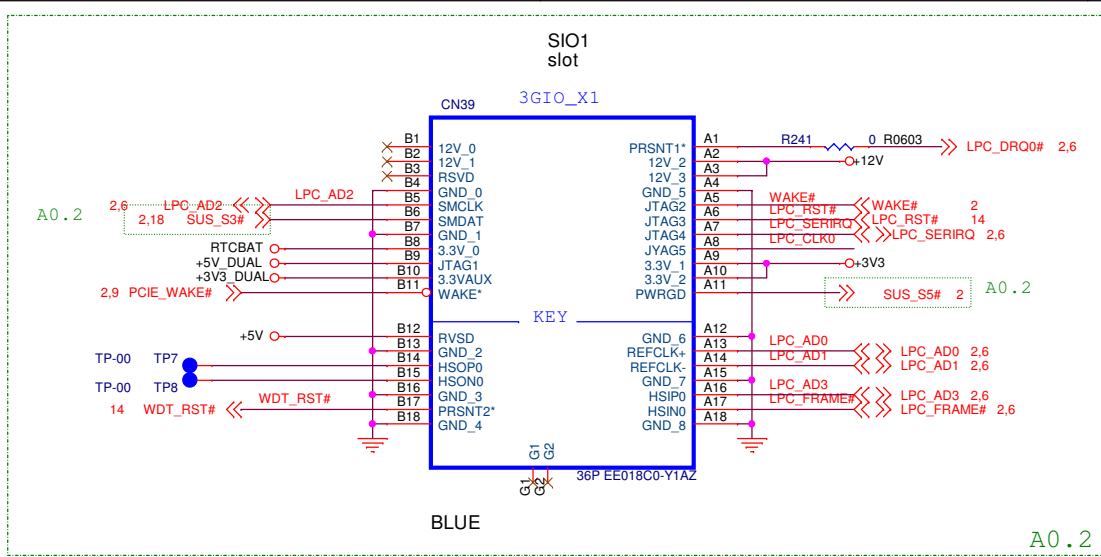
A0.2



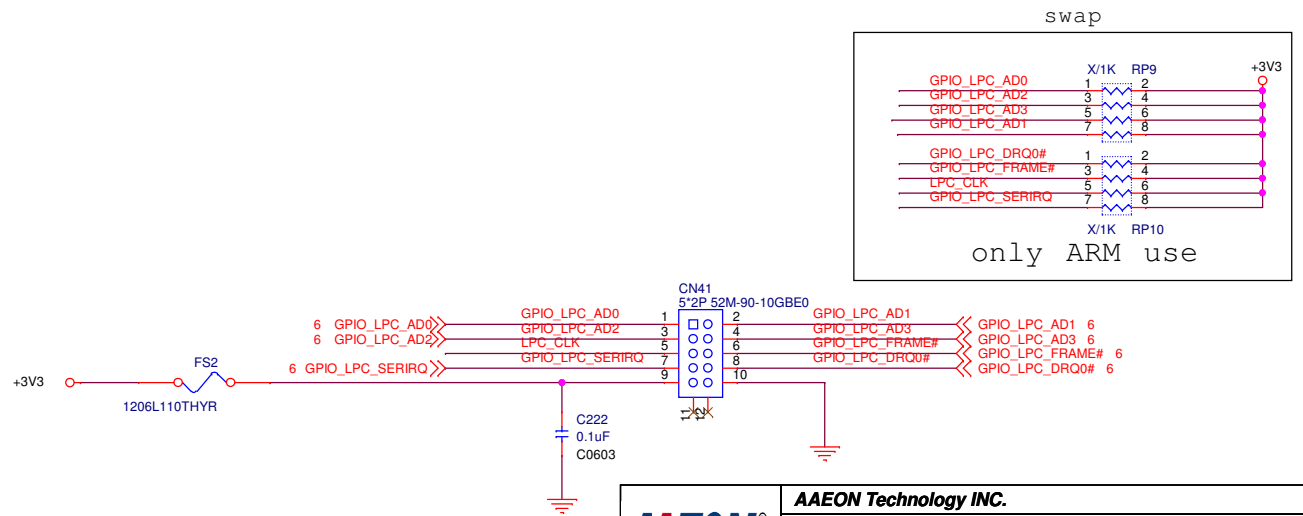
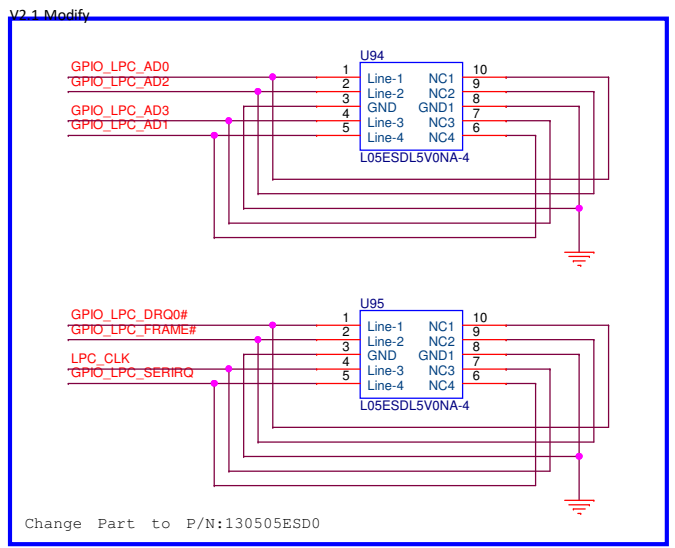
A0.2

$0.34 * \text{CAP}(\text{pF}) = (\text{uS})$
 $0.34 * 10^3 (\text{uS}) = 340\text{uS}$

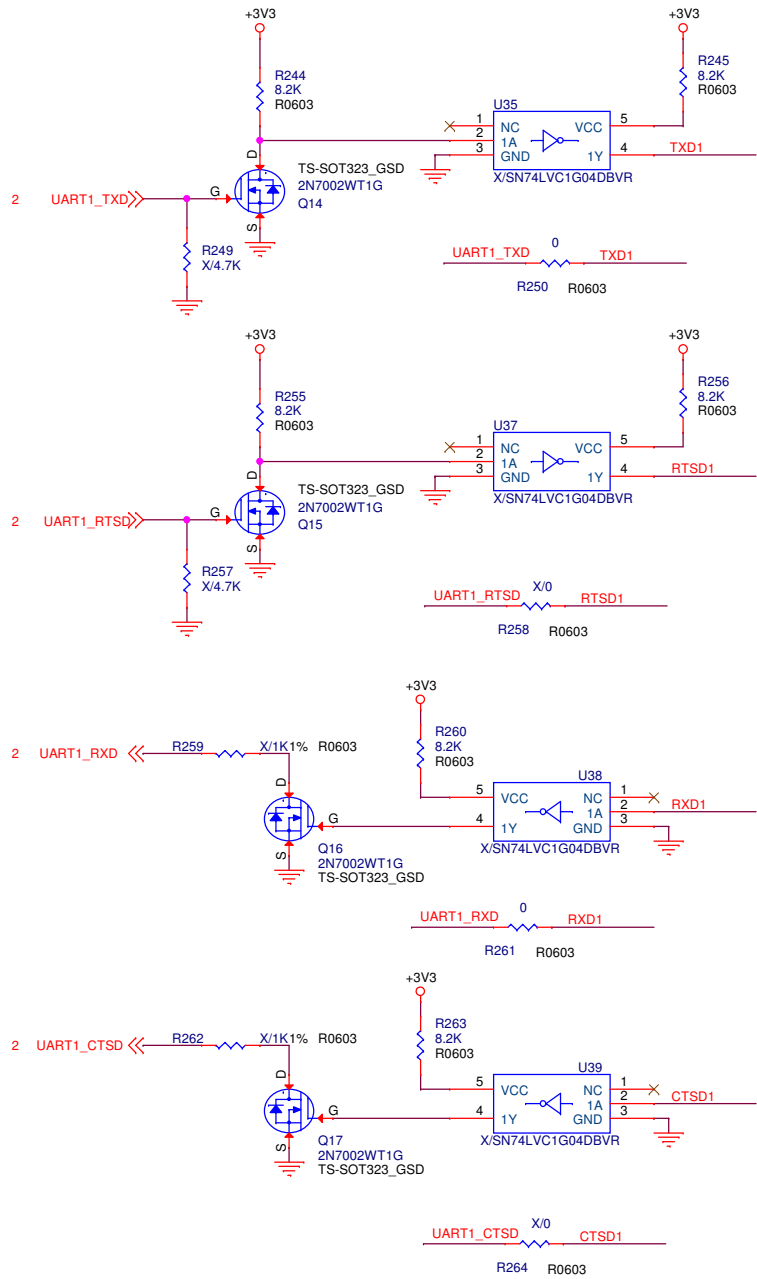
 An ASUS Company		AAEON Technology INC.	
		Title RESET + PWROK	
Size B	Document Number ECB-970	Rev A2.0_0_0	
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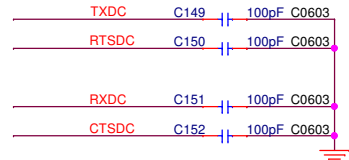
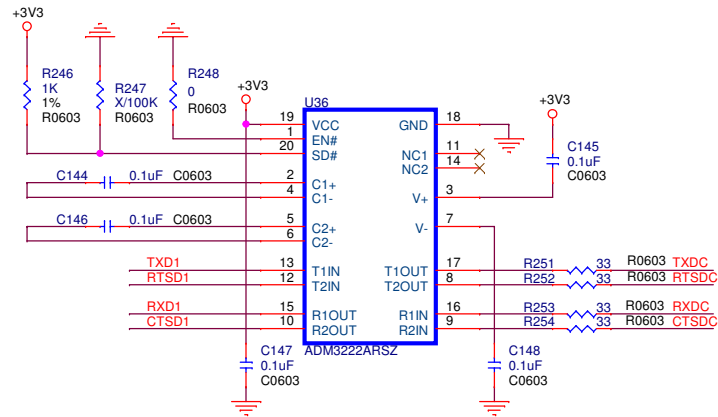
GEN E CV0 5 A0 2



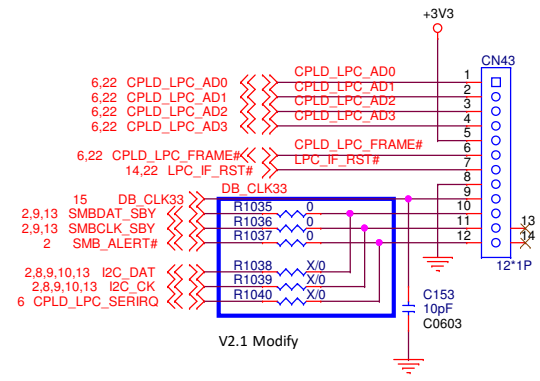
AAEON Technology INC.		
Title SIO Card SLOT		
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A0.2

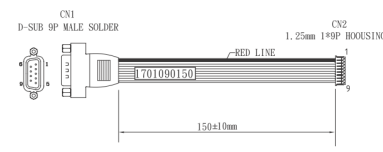
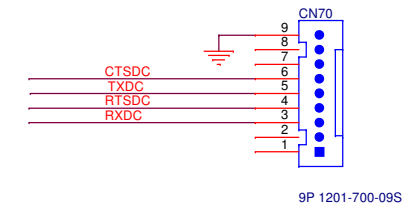


LPC Debug Port & Expansion



V2.1 Modify

腳位	簡寫	意義	說明
Pin1	CD	Carrier Detect	數據機通知電腦有載波偵測到。
Pin2	RXD	Receiver	接收資料。
Pin3	TXD	Transmit	傳送資料。
Pin4	DTR	Data Terminal Ready	電腦告訴數據機可以進行傳輸。
Pin5	GND	Ground	地線。
Pin6	DSR	Data Set Ready	數據機告訴電腦一切準備就緒。
Pin7	RTS	Request To Send	電腦要求數據機將資料送出。
Pin8	CTS	Clear To Send	數據機通知電腦可以傳資料過來。
Pin9	RI	Ring Indicator	數據機通知電腦有電話進來。



線材:UL 2651 FLAT CABLE P=1.0mm

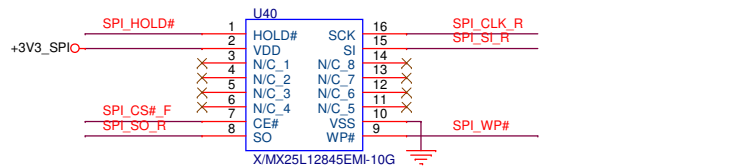
CN1	1	2	3	4	5	6	7	8	9
CN2	1	3	5	7	9	2	4	6	8
COLOR	RED	GRAY	GRAY	GRAY	GRAY	GRAY	GRAY	GRAY	GRAY

RoHS Compliant

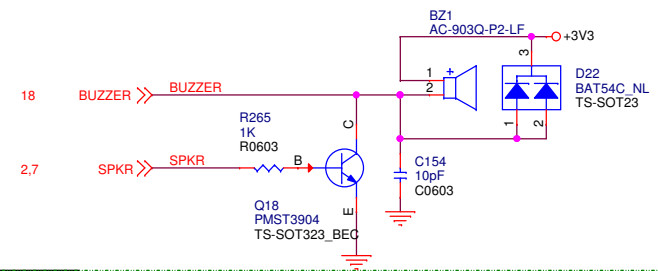
CUST.P/N:1701090150
P/N:A003-709
凱迅電子有限公司

		AAEON Technology INC.	
		Serial port + LPC	
Size B	Document Number ECB-970		Rev A2.0_0.0
Date: Friday, March 09, 2018		Sheet 16 of 24	

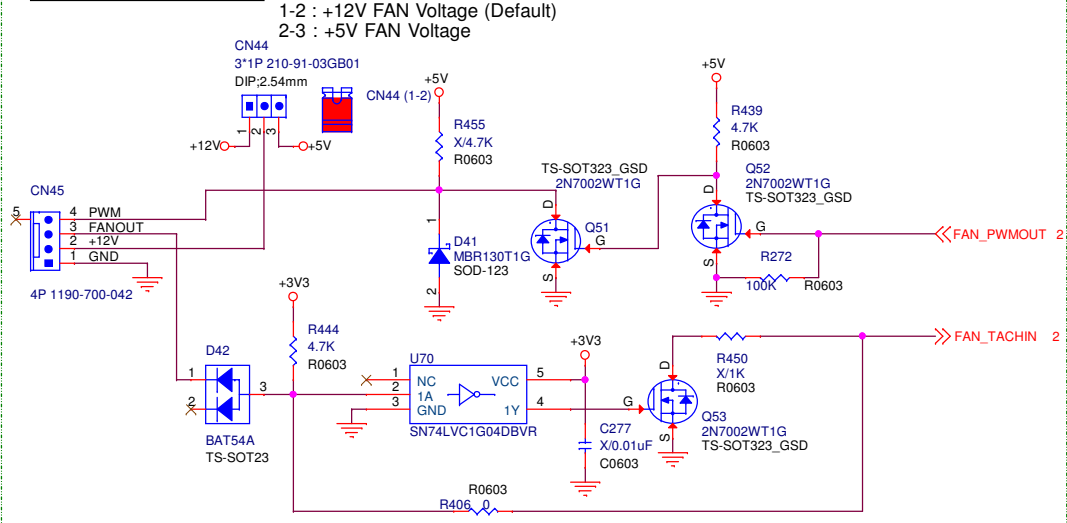
SPI



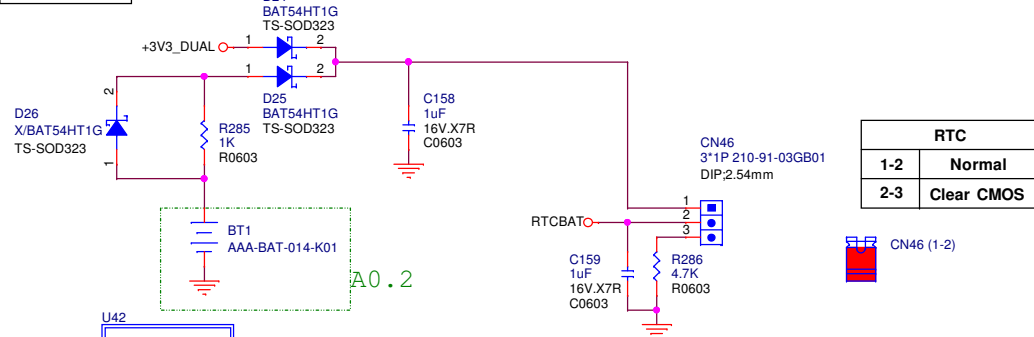
Buzzer



PWM FAN Control



RTCBAT



RTC	
1-2	Normal
2-3	Clear CMOS

AAEON Technology INC.

SPI + Buzzer + FAN + RTC

Document Number: **ECB-970**

Rev: **A2.0_0_0**

Date: Friday, March 09, 2018

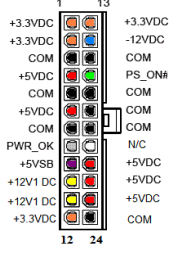
Sheet 17 of 24



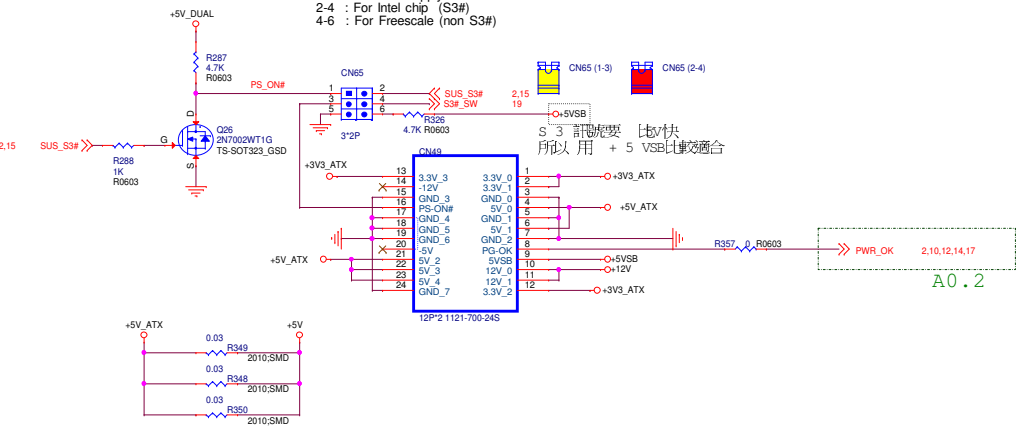
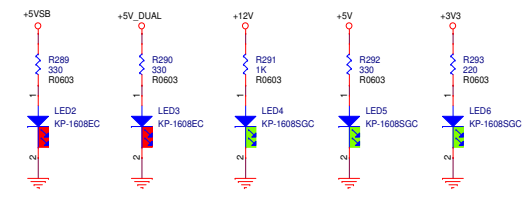
1-3 : For ATX supply controlled (Default)
 3-5 : For ATX supply in AT mode
 2-4 : For Intel chip (S3#)
 4-6 : For Freescale (non S3#)

S3 許認要 比快
 所以用 +5 VSB比較適合

POWER CONNECTOR

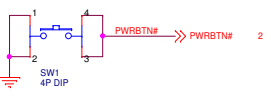


POWER LED

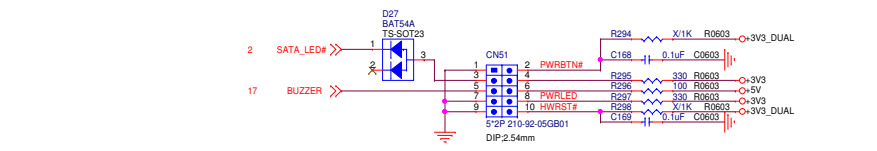
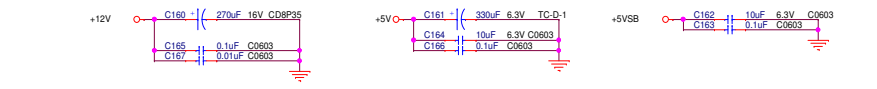
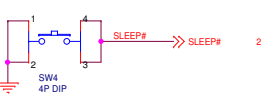
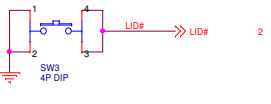
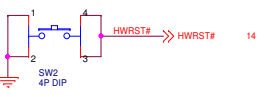


PWR_OK 2,10,12,14,17
 A0.2

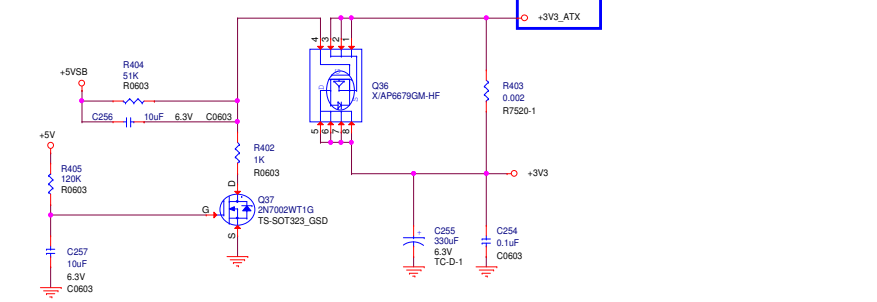
POWER BUTTON



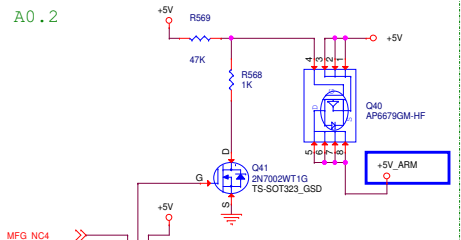
RESET BUTTON



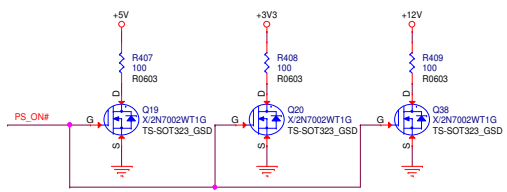
+3.3V Circuit



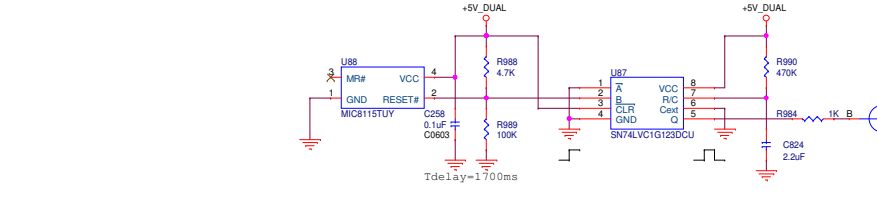
A0.2



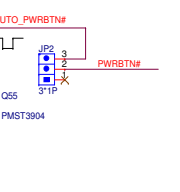
ARM Standby Voltage Selection
 1-2 : X86 Always on (Default)
 2-3 : ARM CTRL

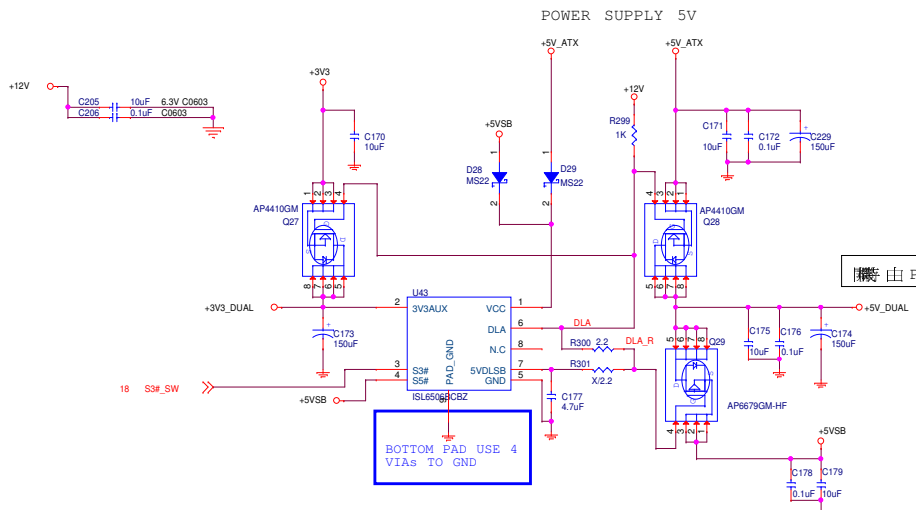


A1.0



JP2(3-3) 1653-MJ-00 Black





Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply Current	I _{SVSB}	V _{S3#} = 5V, V _{SS5#} = 5V (S0 State)	-	3.60	-	mA
		V _{S3#} = 0V, V _{SS5#} = 5V (S3 State)	-	4.60	-	mA
		V _{SS#} = 0V (S5 State)	-	4.60	-	mA

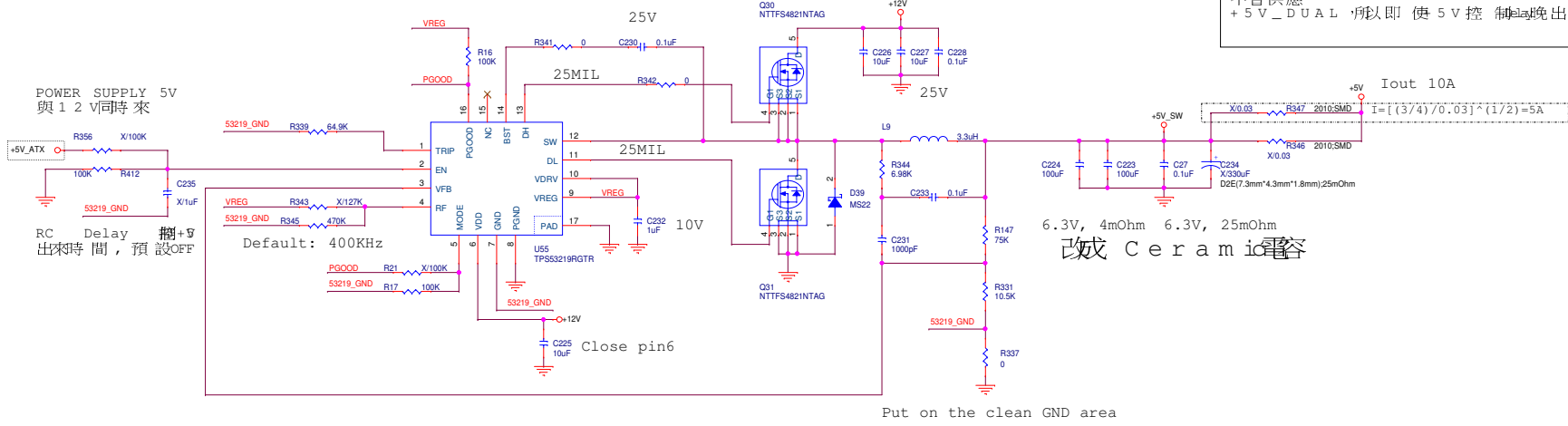
The DLA pin is forced to a high impedance state which allows the 12V rail to enhance the two N-MOSFETs

續由 POWER SUPPLY 供應

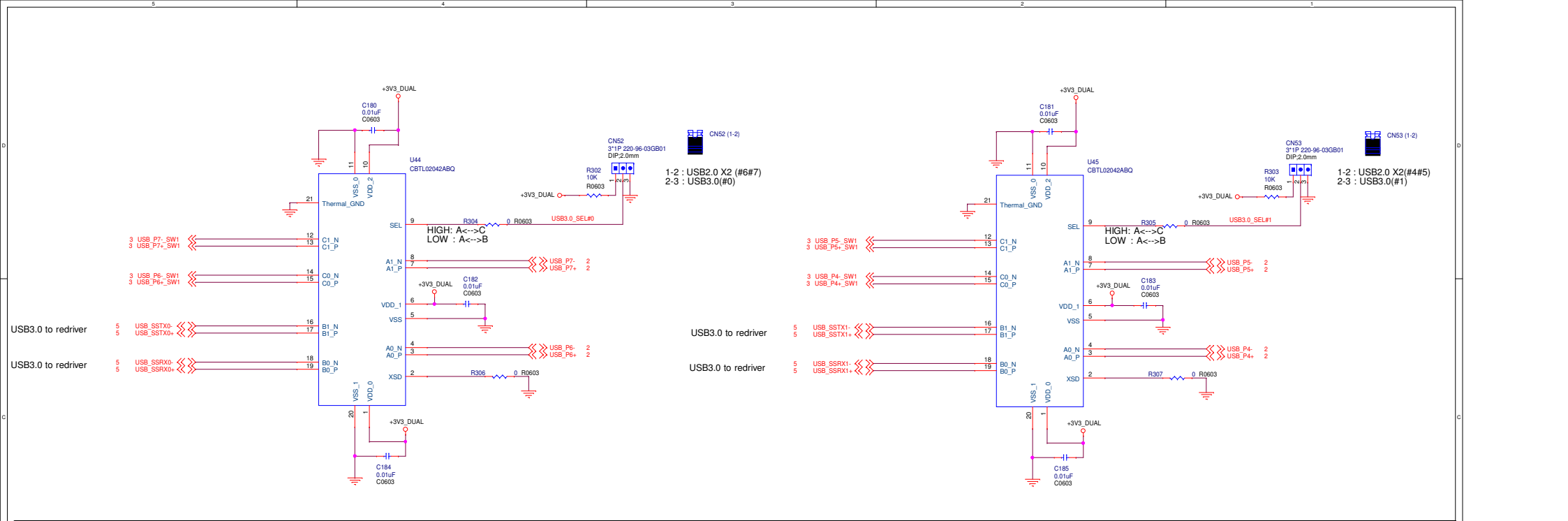
12V >> 5V 暫

改 131520031 2

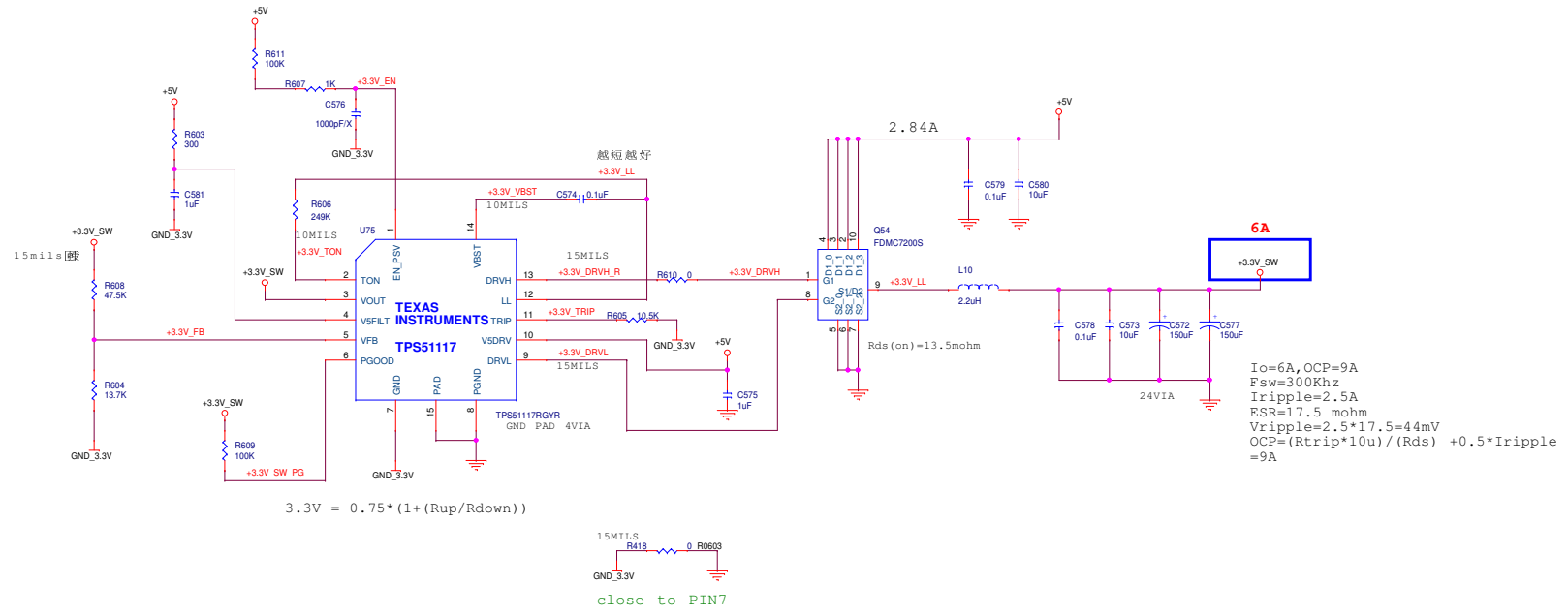
不會供應 +5V_DUAL 所以即使 5V 控制 輸出 也不會影響 u 切換

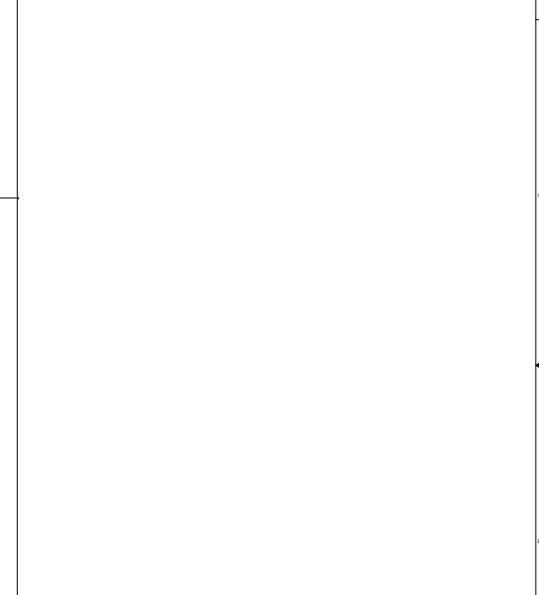
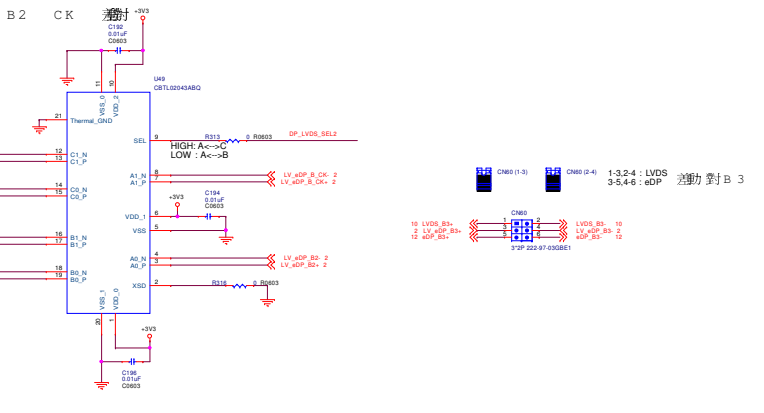
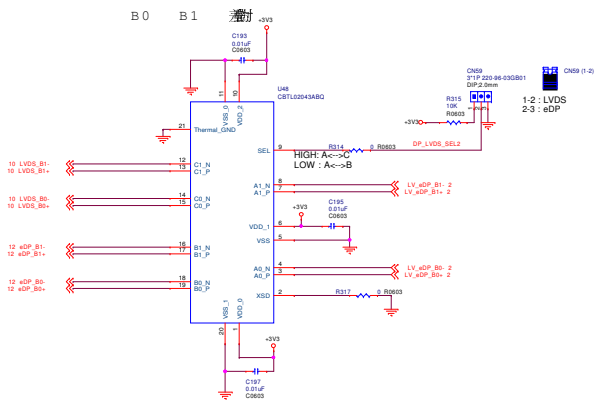
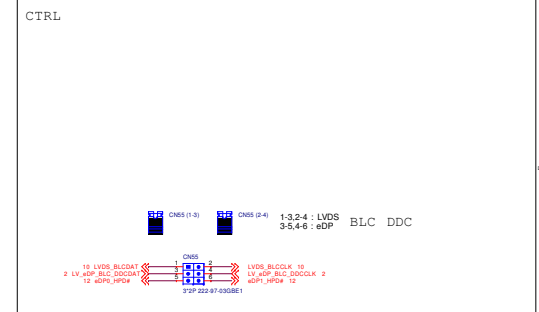
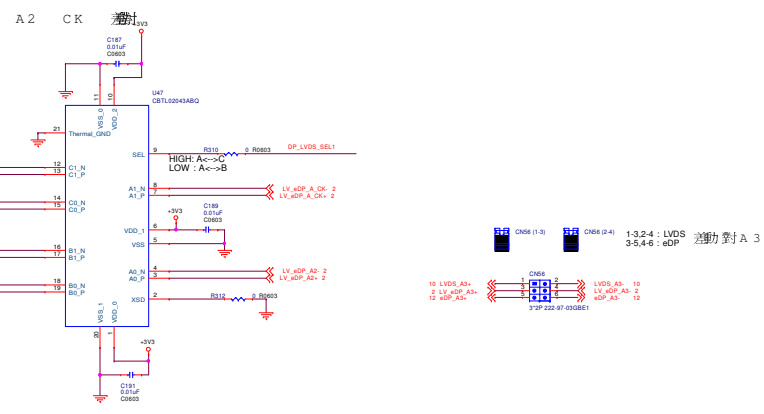
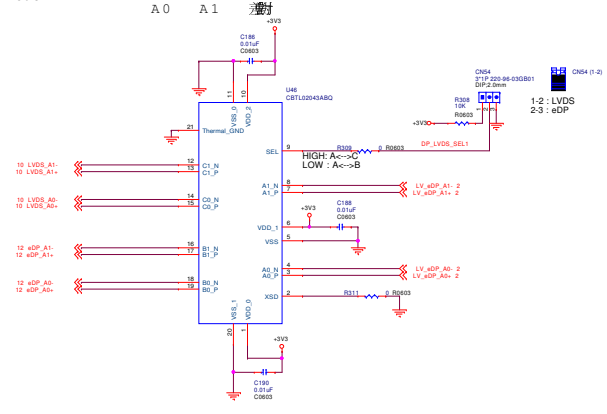


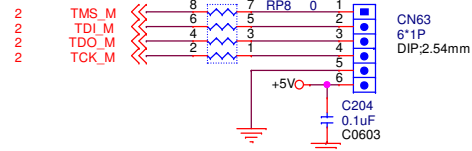
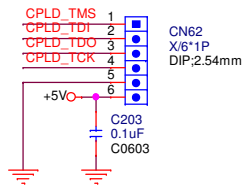
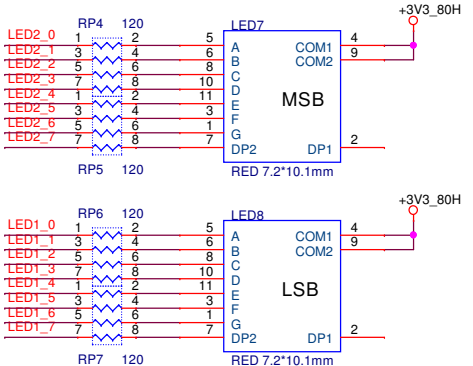
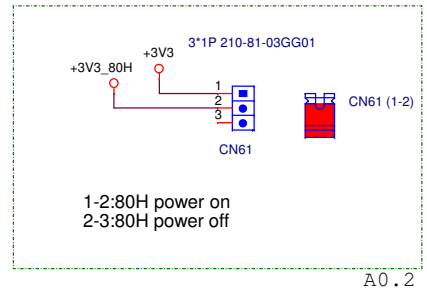
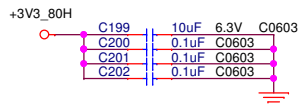
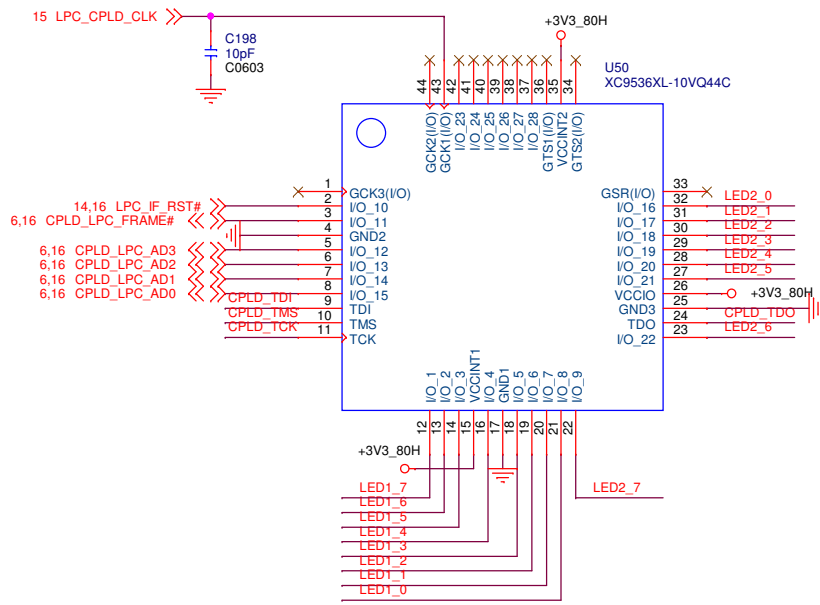
6.3V, 4mOhm 6.3V, 25mOhm
改 Ceramic 電容




A1.0





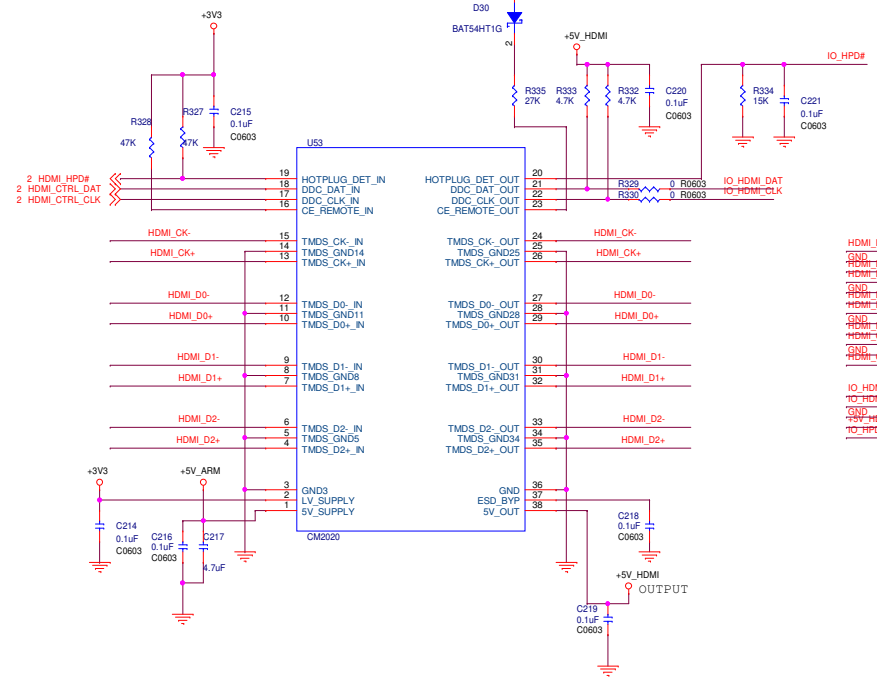
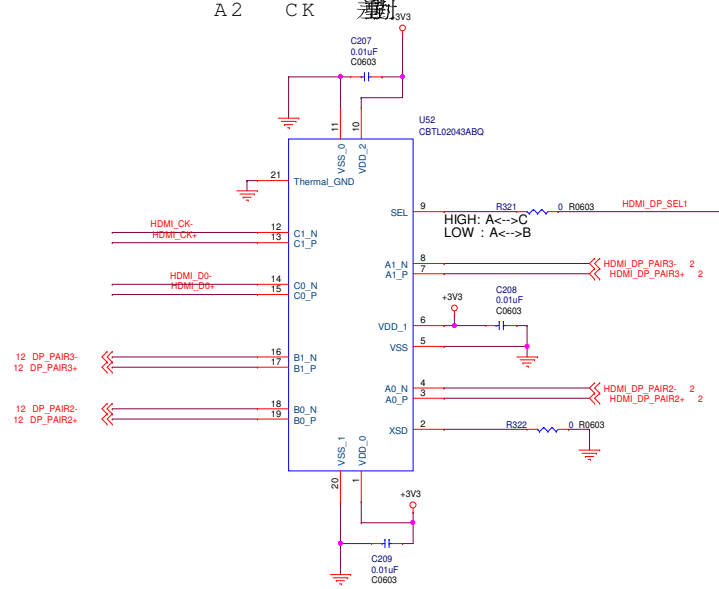
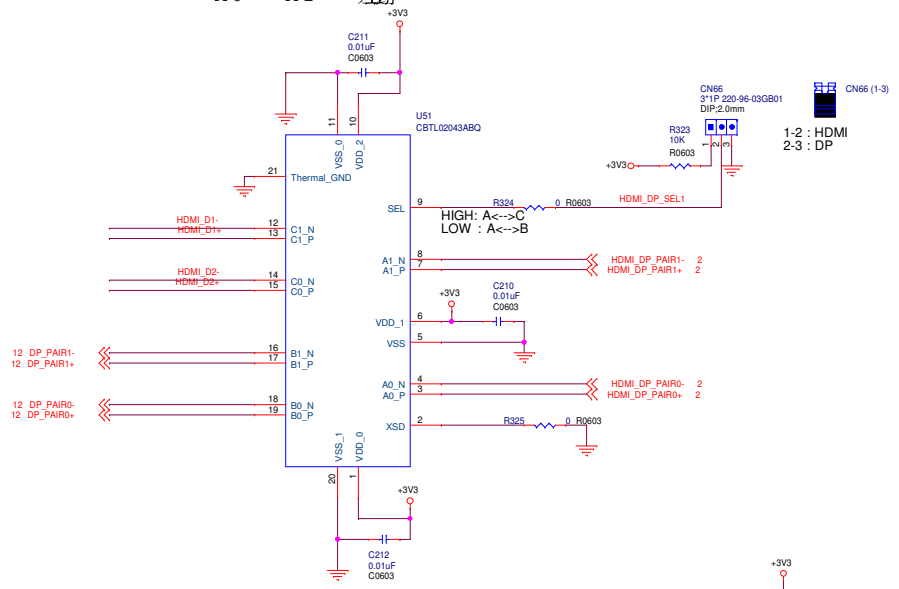


AQ7-LN CPLD

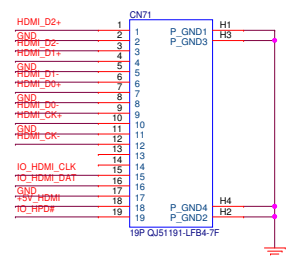
 AAEON An ASUS Company		AAEON Technology INC.	
		Title: LPC 80H	
Size: B	Document Number: ECB-970		Rev: A2.0_0_0
Date: Friday, March 09, 2018		Sheet: 22	of: 24

A0 A1 差動

A2 CK 差動



A0.2 換 Connect α



- 2012/11/15 - change LVDS CN31 向
- 2012/11/15 - change SUPER IO SOLT CN39 繼
- 2012/11/15 - P2 VCC 繼誤已修正
- 2012/11/15 - P18 給switch S3 的5 加上
- 2012/11/15 - 加上LVDS與P的SWI 以及 損
- 2012/11/15 - P7 P8 POWER OFF 繼誤
- 2012/11/16 - (#4-#7)改 B Y 4 U 繼誤
- 2012/11/16 - USB3.0 假地RD使用3A/30ohm/0 0 M
- 2012/11/16 - P2 VCC 繼成1 假 留一個DUA 改或 6
- 2012/11/16 - P15 P07 P08 相時繼誤
- 2012/11/19 - P19 +5V_SB 改+5V
- 2012/11/20 - P15 SIO SLOT 假
- 2012/11/21 - P11 CN33 繼誤
- 2012/11/21 - P19 CN50繼
- 2012/11/22 - P22 CN61 OFF 繼誤
- 2012/11/22 - P11 CN33 改ootprint
- 2012/11/22 - P15 繼 拿掉 pull 繼留
- 2012/11/22 - P7 SW 繼 預留DIS繼留阻
- 2012/11/22 - P2 繼及銅柱
- 2012/11/27 - P19 12V>>5V留
- 2012/11/29 - P03 繼GN 修改
- 2012/11/29 - P07 繼 Audio IO power
- 2012/11/30 - LVDS I2C SMBUS 繼 FUSEr

A0.2

- P03 繼 U 繼留能
- P04 USB OTG 假
- P07 左繼繼繼繼
- P07 Audio Connector 繼
- P07 繼 r1 繼
- P11 D19繼
- P12 繼eD P Connecto r 與 Backlight pow
- P13 繼CAN BUS LEVE L SHIFT,CN置換Connect
- P14 R358 繼
- P15 SIO SLOT 繼或A假定義
- P23 CN71繼Connector

A1.0

- P03 R7,R9 >> 2.2K繼
- P04 繼D17,D1 8 繼 件
- P10 LVDS Backlight power 繼新增R414,R410,R411,繼阻,新 增CN 67 LVDS C繼or與切換電阻R583-R602
- P12 繼fsl 1 ,U換成14S3524700
- P13 CN57繼Connector
- P14 R230 繼
- P16 R264 繼, R2 繼
- P17 R450 繼, R4 繼
- P18 繼AUTO POWE R BUTT繼路
- P19 繼R4 繼阻 繼阻 繼不件, R345 繼阻改 470Ω30與Q31 MS 繼或
- P20 繼U75 POWER FOR 3.3V
- P22 LED7與ED8 繼

A2.0

- CN1的in1繼增加J繼來選擇P00或是原的 STAT#
- CN1的in2繼增加J繼來選擇PI1或是原的 SW#
- CN1的in2繼增加J繼來選擇PI2或是原的 EDW#
- CN1的in5繼增加J繼來選擇繼ved或是原的D IO _D 繼
- CN1的in5繼增加J繼來選擇繼ved或是原的D IO _D 繼
- CN1的in5繼增加J繼來選擇繼ved或是原的D IO _D 繼
- CN1的in5繼增加J繼來選擇繼ved或是原的D IO _D 繼
- CN1的in2 繼增加J繼來選擇PIO 或是原的 繼
- CN1的in13繼增加USB_SST X-
- CN1的in13繼增加USB_SST X+
- CN1的in14繼增加USB_SS R X-
- CN1的in14繼增加USB_SS R X+
- CN1的in211~Pin218繼增加J繼來繼繼NC或 原VCC
- 繼micr o s
- 繼GP0和繼切換S with IC
- 繼繼繼繼繼 繼件繼
- 繼VGA_GND和GND_CHASS 繼直接 接到
- Change U19, U22, U25 P/N:130505ESD0
- Change D31-D38 to U94, U95, components P/N:130505ESD0
- Change CN68, CN9, CN8, CN74 繼繼繼繼繼
- Change CN57(2-3) and CN58(2-3) for LPC mode